Next Generation Silicon Photonic Transceiver: From Device Innovation to System Analysis

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ABSTRACT

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Silicon photonics is recognized as a disruptive technology that has the potential to reshape many application areas, for example, data center communication, telecommunications, high-performance computing, and sensing. The key capability that silicon photonics offers is to leverage CMOS-style design, fabrication, and test infrastructure to build compact, energy-efficient, and high-performance integrated photonic systems-on-chip at low cost. As the need to squeeze more data into a given bandwidth and a given footprint increases, silicon photonics becomes more and more promising. This work develops and demonstrates novel devices, methodologies, and architectures to resolve the challenges facing the next-generation silicon photonic transceivers.

The first part of this thesis focuses on the topology optimization of passive silicon photonic devices. Specifically, a novel device optimization methodology - particle swarm optimization in conjunction with 3D finite-difference time-domain (FDTD), has been proposed and proven to be an effective way to design a wide range of passive silicon photonic devices. We demonstrate a polarization rotator and a 90° optical hybrid for polarization-diversity and phase-diversity communications - two important schemes to increase the communication capacity by increasing the spectral efficiency.

The second part of this thesis focuses on the design and characterization of the next-generation silicon photonic transceivers. We demonstrate a polarization-insensitive WDM receiver with an aggregate data rate of 160 Gb/s. This receiver adopts a novel architecture which effectively reduces the polarization-dependent loss. In addition, we demonstrate a III-V/silicon hybrid external cavity laser with a tuning range larger than 60 nm in the C-band on a silicon-on-insulator platform. A III-V semiconductor gain chip is hybridized into the silicon chip by edge-coupling to the silicon chip. The demonstrated packaging method requires only passive alignment and is thus suitable for

high-volume production. We also demonstrate all silicon-photonics-based transmission of 34 Gbaud (272 Gb/s) dual-polarization 16-QAM using our integrated laser and silicon photonic coherent transceiver. The results show no additional penalty compared to commercially available narrow linewidth tunable lasers.

The last part of this thesis focuses on the chip-scale optical interconnect and presents two different types of reconfigurable memory interconnects for multi-core many-memory computing systems. These reconfigurable interconnects can effectively alleviate the memory access issues, such as non-uniform memory access, and Network-on-Chip (NoC) hot-spots that plague the many-memory computing systems by dynamically directing the available memory bandwidth to the required memory interface.

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Glossary

16-QAM	16-ary Quadrature Amplitude Modulation
ACK	Acknowledgement
AR	Anti-Reflective
ASE	Amplified Spontaneous Emission
ASIC	Application-Specific Integrated Circuit
AWG	Arrayed Waveguide Grating
BER	Bit Error Rate
BOX	Buried Oxide
BPM	Beam Propagation Method
CDR	Clock and Data Recovery
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chip Multiprocessor
CPU	Central Processing Unit
CW	Continuous-Wave
CWDM	Coarse Wavelength-Division Multiplexing
DAC	Digital-to-Analog Converter
DC	Directional Coupler
DCA	Digital Communications Analyzer
DCI	Datacenter Interconnect
DMM	Digital Multimeter
DP	Dual-Polarization
DRAM	Dynamic Random-Access Memory
DSP	Digital Signal Processor
DWDM	Dense Wavelength Division Multiplexing
ECL	External Cavity Laser
EDA	Electronic Design Automation
EDFA	Erbium-Doped Fiber Amplifier
EIM	Effective Index Method
EO	Electro-Optical
FDTD	Finite-Difference Time-Domain
FEM	Finite Element Method
FPGA	Field-Programmable Gate Array
FSR	Free Spectral Range
GC	Grating Coupler
HBM	High Bandwidth Memory
HMC	Hybrid Memory Cube
HPC	High-Performance Computing
HR	High Reflectivity
IMRA	Integrated Modulator/Receiver Assembly
InP	Indium-Phosphide
IO	Input/Output
IoT	Internet-of-Things
IP	Intellectual Property
ITLA	Integrated Tunable Laser Assembly
LA	Limiting Amplifier
LIV	Light-Current-Voltage
MCM	Multi-Chip Module
MFD	Mode-Field Diameter
MMI	Multimode Interference
MPD	Monitoring Photodetector
MPW	Multi-Project Wafer
MQW	Multi-Quantum-Well

MZ Mach-Zehnder

MZI Mach-Zehnder Interferometer

NoC Network-on-Chip

NRZ Non-Return-to-Zero

NUMA Non-Uniform-Memory-Access

OCMM Optically Connected Memory Module

OOK On-Off Keying

OSA Optical Spectrum Analyzer

OSNR Optical Signal-to-Noise Ratio

PC Polarization Controller

PCE Polarization Conversion Efficiency

PD Photodetector

PDK Process Design Kit

PDWS Polarization-Dependent Wavelength Shift

PIC Photonic Integrated Circuit

PM Polarization Maintaining

PMD Polarization Mode Dispersion

PPG Pulsed-Pattern Generator

PR Polarization Rotator

PRBS Pseudo-Random Binary Sequence

PS Polarization Scrambler

PSM Parallel Single-Mode

PSO Particle Swarm Optimization

PSR Polarization Splitter and Rotator

QAM Quadrature Amplitude Modulation

QPSK Quadrature Phase-Shift Keying

QSFP Quad Small Form-factor Pluggable

RSOA Reflective Semiconductor Optical Amplifier

Rx Receiver

SiN Silicon Nitride

SiPh Silicon Photonics

SISCAP Silicon Insulator Silicon Capacitor

SMF Single Mode Fiber

SMSR Side-Mode Suppression Ratio

SOI Silicon on Insulator

SOP State of Polarization

SPP Surface Plasmon Polariton

SSC Spot-Size Converter

SST Structural Simulation Toolkit

SWG Subwavelength Grating

SYN Synchronization

TDM Time-Division Multiplexing

TE Transverse Electric

TIA Trans-Impedance Amplifier

TL Tunable Laser

TM Transverse Magnetic

TO Thermo-Optic

Tx Transmitter

VOA Variable Optical Attenuator

WDM Wavelength-Division Multiplexing

WPE Wall-Plug Efficiency

WSR Wavelength-Selective Reflector

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Chapter 1

Introduction

1.1 Silicon Photonics in the Zettabyte Era

We are living in an era when there is an exponentially increasing amount of information being handled by the Internet due to the emergence of the Internet-of-Things (IoT) and Cloud technologies [1]. Based on Cisco's statistics and predictions [2], the global IP traffic was 1.2 Zettabyte in 2016 and will increase nearly threefold from 2016 to 2021. The rapid growth in the demand for data transmission capacity has driven the development of optical transmission systems with high spectral efficiency, high energy efficiency, and low cost [3].

Silicon photonics is one of the promising technologies for the next-generation optical interconnects. It has the potential to reshape many application areas, for example, data center communication, high-performance computing, telecommunications, and sensing [4]. The reason is that silicon photonics can leverage CMOS-style design, fabrication, and test infrastructure to build compact, energy-efficient, and high-performance integrated photonic systems at low cost [5, 6].

The potential of silicon photonics was first recognized in the studies of waveguides in Silicon-on-Insulator (SOI) wafers in 1985 [7, 8, 9]. A significant amount of research on the reduction of waveguide loss [10, 11] was undertaken in the late eighties and early nineties. In 1991, Soref et al. [10] proposed Eq. 1.1 to determine the necessary cross-sectional dimensions for a single-mode rib waveguide, where a and b are related

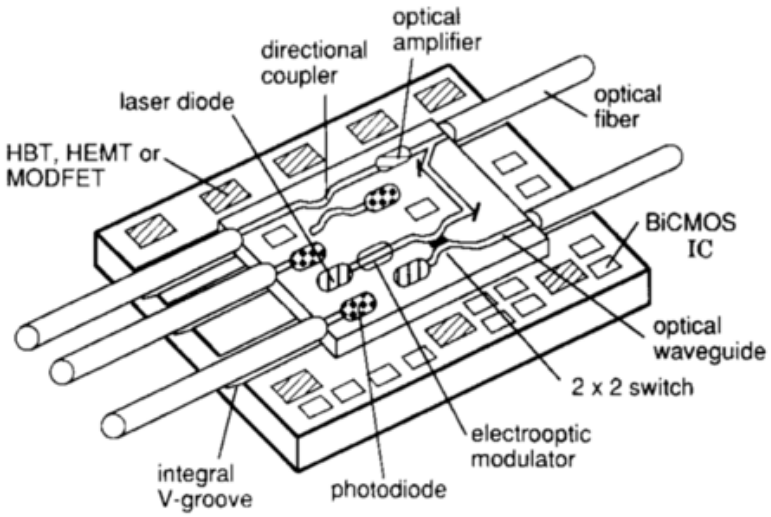


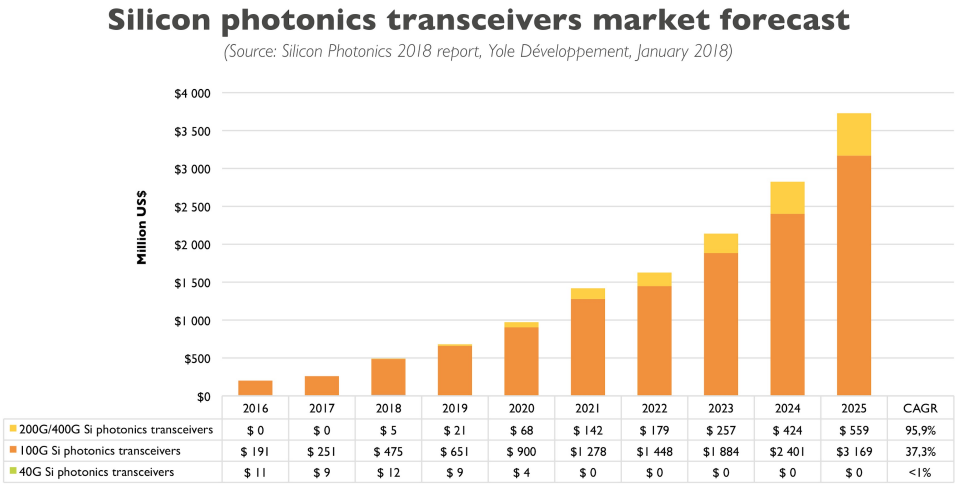
Figure 1.1: Silicon-based optoelectronic superchip. (adapted from [13])

to the rib width and inner rib height, and r is the outer-inner ratio.

$$\frac{a}{b} \leq 0.3 + \frac{r}{\sqrt{1-r^2}} \tag{1.1}$$

In 1992, Abstreiter first proposed the fully integrated monolithic optoelectronic "superchip" for silicon hybrid integration [12]. The superchip incorporates all the functionalities of optical communications, including the creation, routing, amplifying, detection and so forth of the optical signal. The optical fibers were butt-coupled to the photonic chip, which could subsequently be integrated with the electrical chip [13]. Under the guidance of this vision, a myriad of optoelectronic devices have been developed, including high-speed modulators [14, 15, 16], Ge- and SiGe-based photodetectors [17, 18, 19, 20], micro-ring modulators [21, 22], WDM filters [23, 24], grating/edge couplers [25, 26, 27, 28, 29], phase shifters [30, 31], and reconfigurable electro-optic (EO)/thermo-optic (TO) switches and routers [32, 33, 34, 35].

The functionalities of silicon photonics can be further enhanced and extended by integrating silicon with other materials, including graphene, silicon nitride, III-V compound semiconductors, other group-IV elements like Ge, and magneto-optical materials. For example, graphene-based high-speed EO modulators and photodetectors have been demonstrated [36, 37, 38, 39, 40, 41]. SiN-on-SOI platforms open the possibility for passive optical functionalities implemented in the SiN layer to be combined with active



	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	CAGR
200G/400G Si photonics transceivers	$ 0	$ 0	$ 5	$ 21	$ 68	$ 142	$ 179	$ 257	$ 424	$ 559	95,9%
100G Si photonics transceivers	$ 191	$ 251	$ 475	$ 651	$ 900	$1 278	$1 448	$1 884	$2 401	$3 169	37,3%
40G Si photonics transceivers	$ 11	$ 9	$ 12	$ 9	$ 4	$ 0	$ 0	$ 0	$ 0	$ 0	<1%

Figure 1.2: Silicon photonic transceiver market forecast. (adapted from [63])

functionalities in the SOI [42, 43]. The III-V compound materials are used to create lasers and provide gain [44, 45, 46, 47, 48, 49]. Magneto-optic materials are used to form non-reciprocal photonic devices like isolators and circulators [50, 51, 52].

In the early 2000s, the commercialization of silicon photonic transceivers started. Companies like Luxtera [53, 54, 55] and Kotura [19, 56] first introduced their products to the market. Recently, other companies like Intel [57, 58, 59], Cisco [60, 61], Acacia [62] joined in and started shipping their silicon photonic transceiver products in high volume for the high-performance computing (HPC), datacenter interconnect (DCI), and telecommunications optical transport markets.

1.2 Silicon Photonic Transceivers

According to Yole's report [63], the silicon photonic technology has reached its tipping point, with transceivers shipping in volume, as shown in Fig. 1.2. The main driving force behind it is the anticipated large-scale deployment of silicon photonic transceivers in the mega-datacenter and high-performance computing companies, as the cost drops to $1/Gbps.

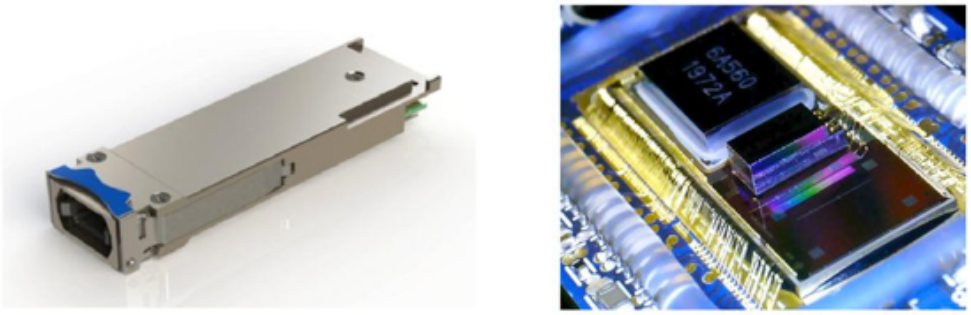


Figure 1.3: (a) QSFP28 form factor module (b) Chipset internal to QSFP28 module, the picture shows the assembled ICs and their assembly on the PCBA. (adapted from [55])

1.2.1 Data Center and High-Performance Computing

Data center bandwidth requirements increase with the growing popularity of video streaming, cloud computing, and other data intensive applications. There is a growing demand for longer reach optical links in intra- and inter-datacenter interconnects (from 500 m to 80 km) for datacenter expansion or installation of new mega-datacenters [64, 65, 66]. The use of single-mode fiber infrastructure for newly installed mega-datacenters, or interconnects between datacenters, open promising opportunities for silicon photonic integration [67].

A series of silicon photonic short reach transceivers have been demonstrated and are available on the market [68]. One popular solution is based on parallel single-mode fibers (PSM), and the other is based on wavelength-division multiplexing (WDM). Intel [69], Cisco [61], and many other companies all demonstrated their silicon photonic transceivers. Fig. 1.3 shows Luxtera's silicon-photonics-based 100 Gbps (4x26 Gbps) transceivers for parallel single mode fiber communication.

1.2.2 Telecommunications

Until circa 2002, fiber-optic communication deployed for long-haul distance (600-15,000 km) and metropolitan distance (80 - 600 km) used mostly on-off keying (OOK) transmission [70]. As the traffic capacity kept growing, it became too expensive to install new optical fibers to support the OOK transmission. As a result, carriers and datacenter operators shifted focus to coherent systems, because coherent systems offer much

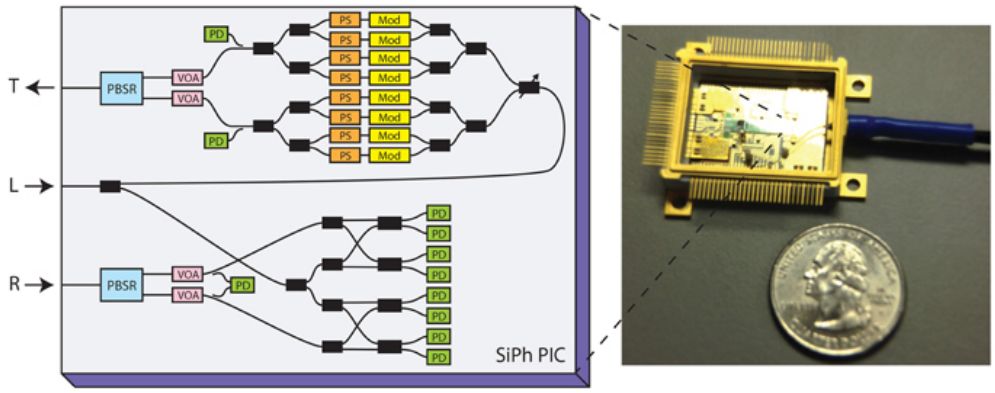


Figure 1.4: Block diagram of a silicon single chip transceiver excluding laser. Gold box with the silicon PIC packaged with drivers, transimpedance amplifiers, fiber array, and other components. (adapted from [79])

higher bit rates by using more advanced modulation formats [71, 72, 73, 74].

100Gb/s coherent systems have been widely deployed, as the price, footprint, and power consumptions of such systems keep decreasing. To meet these tight requirements, people must use photonic integration. Acacia [75, 76], Cisco [60, 77], Bell Labs [78], and many other companies all demonstrated their silicon photonic coherent transceivers. Fig. 1.4 shows Acacia's silicon-photonics-based coherent transceiver. The transceiver includes 4 carrier-depletion Mach-Zehnder modulators, 4 pairs of high speed Germanium photodiodes (PDs), 2 sets of 90° optical hybrid, 3 fiber couplers, 2 polarization beam splitter and rotators (PBSRs), and many splitters, thermo-optic phase shifters (PSs), variable optical attenuators (VOAs), monitor diodes (PDs), and routing waveguides [79].

1.3 Key Components for Silicon Photonic Transceivers

The design of silicon photonic transceivers (or, more broadly, any complicated silicon photonic system) needs to start from the design of the very basic devices [80, 81, 82, 83, 84, 85]. Thus, a review of recent progress in silicon photonic passive and active devices is provided in this section.

1.3.1 Passive Devices

1.3.1.1 Fiber-to-Chip Light Couplers

Coupling light into/out of a high index-contrast silicon waveguide from/into a single mode fiber (SMF) with a mode-field diameter (MFD) larger than 5 μm is a non-trivial problem because of the high coupling loss due to the severe modal field and effective index mismatch. Two devices - edge couplers and grating couplers are often used to address this issue.

Edge couplers, also known as spot-size converters (SSCs) are used to covert the highly confined mode ($\sim$ 0.5 μm $\times$ 1 μm) in the Si waveguide to a much larger fiber mode ($\sim$ 10 μm $\times$ 10 μm). The typical method is to use a single-stage inverse taper [86, 87], as known as nano-taper, in which the waveguide is gradually narrowed down to a very small size in a suspended glass waveguide [88, 89, 90] or a knife-edge waveguide [91]. Edge couplers with large misalignment tolerance like the trident SSCs [92, 93] and SSCs with the deposition of low-index material overlay over the inverse taper [94] have also been demonstrated.

Grating couplers, also known as surface-emitting grating couplers reflect light to enter (or emit from) the surface of the wafer at a roughly 90° angle, are well-suited for inline probing, wafer-level automatic measurement, or coupling to an optical fiber in some real products [95, 96]. The typical grating couplers are formed using either through-etched trenches or shallow-etched trenches [97, 98, 99]. Methods such as utilizing embedded metal mirrors [96, 100], polysilicon overlay [101], and sub-wavelength structures [102, 103, 104] to improve the efficiency and directionality of the grating couplers have also been demonstrated.

1.3.1.2 Power Dividers and Combiners

Power dividers/combiners are used to split/combine optical signals. Commonly used power dividers/combiners include multimode interferometer (MMI) [105, 106, 107], Y junctions [108, 109], and directional couplers (DC)[110]. More recently, adiabatic 3dB couplers and MMI couplers [111, 112, 113, 114] have been demonstrated to have more compact footprint, larger bandwidth, and larger fabrication tolerance. In addition to uniform power splitting ratios, any arbitrary splitting ratio can be achieved [115, 116, 117].

1.3.1.3 Filters

Optical filters are extensively used in optical interconnect systems to performance signal processing and wavelength division multiplexing. Most commonly used filters include arrayed waveguide gratings (AWG) [118, 119, 120, 121, 122], Echelle gratings [123, 124, 125, 126], ring resonators [127, 128, 129, 130, 131, 132], multimode interference [133], and Fabry-Pérot [134, 135, 136]. AWGs have large channel counts and large footprints. For example, a 512 $\times$ 512 AWG was demonstrated with a footprint of 16 mm $\times$ 11 mm [120]. On the contrary, ring-resonator-based filters have very compact footprints, wavelength tunablity, very high-Q factors, and can be used for a moderate number of channel counts [137, 138, 139].

1.3.1.4 Polarization Splitters

Polarization splitters are key components to enable dual-polarization communication. One way to implement on-chip polarization splitting is to use a polarization splitting grating couplers, which combines the functionalities of efficient light coupling and polarization splitting [140, 141, 142, 143, 144]. The other way is to use a separate device, like directional couplers (DCs) and MMIs [145, 146, 147, 148, 149, 150]. A fabrication-tolerant DC-based design has a long coupling length (longer than 100 μm) [145]. Compared to DCs, which requires precise control of a narrow coupling gap, the MMIs based on self-imaging principles have a more compact footprint and are more fabrication tolerant [85].

1.3.1.5 Waveguide Crossings

Waveguide crossings are required when the planar optical routing becomes complex, and there is a need to cross two waveguides. Commonly used methods include polymer and silicon nitride waveguide vertical overlay on inverse tapers [151, 152], subwavelength gratings (SWGs) [153], multimode-interference (MMI) [154, 155, 156, 157], Bloch waves [158, 159], and adiabatic tapers [160, 161]. The vertical overlay approach requires the overlay material to expand the mode, thus having relatively large size and a complex process. The subwavelength grating approach exploits the effective medium principle, which states that different optical materials, combined at subwavelength scales, can be

approximated by an effective homogeneous material [153, 162, 163]. But the SWG-based approach suffers from the fabrication variation. The other three approaches are relatively compact and robust.

1.3.2 Active Devices

1.3.2.1 Modulators

There are many different types of Si-based optical modulator [164, 165]. The most widely adopted modulator is the carrier depletion modulator [166, 167] based on the plasma dispersion effect - the change in silicon's refractive index due to the presence of free carriers [168]. The change in refractive index Δn at 1550 nm is described by:

$$\Delta n = -8.8 \times 10^{-22} \Delta N - 8.5 \times 10^{-18} \Delta P^{0.8} \tag{1.2}$$

where ΔN, ΔP are the change in carrier densities of electrons and holes, respectively. Thus, holes are more effective for providing an index shift. The optical signal is passed through a p-n junction, and the depletion width is modulated by the electrical signal. Carrier depletion modulators can operate at >50 Gb/s, but have a high insertion loss [166, 169, 170]. That is because the imaginary part of the refractive index is also modulated which contributes to the unavoidable high loss. The phase-shifting efficiency, $V_\pi L$ is limited from 0.2 to 2.8 V·cm due to the material properties of Si [166].

MOS-capacitor-type modulators have recently been investigated to circumvent this issue. One type of MOS-capacitor modulators is the silicon-insulator silicon-capacitor (SIS-CAP), which consists of a p-type poly-Si layer, a gate-oxide layer, and a n-type SOI layer. The overlapping region of the poly-Si layer and the SOI layer creates a waveguide that confines the optical modes [171, 172, 173]. The other type is III-V/Si-MOS-capacitor modulator. III-V material provide a large electron-induced refractive-index change due to the large carrier-plasma effect and band-filling effect [174, 175, 176]. Also, the higher electron mobility in III-V materials leads to smaller loss and time delay [177]. High phase-shift efficiency (smaller than 0.1 V·cm) has been demonstrated [178, 179].

SiGe electro-absorption modulators based on Franz-Keldysh effect have attracted a lot of attention recently due to their compact footprint, ultra-low energy consumption [180, 181, 182]. The optical mode is evanescently coupled to the Ge absorption

layer, whose absorption can be controlled through an applied voltage. Other type of modulators like graphene modulators by switching the graphene between a transparent insulator and an absorbing metal [38, 41, 183] have also been demonstrated.

1.3.2.2 Photodetectors

Ge-based waveguide photodetectors are widely used in today's silicon photonic integrated circuits. They usually use a p-i-n configuration, consisting of p-doped silicon on which Ge is grown. Due to the 4% lattice mismatch between Ge and silicon, a thin layer of SiGe is grown first to minimize the dislocations. N-doped Ge is grown on the top. The conventional Ge-based waveguide photodetectors have either vertical or lateral p-i-n junctions, with Ge doping and metal contact on top of Ge [20, 184, 185, 186, 187, 188, 189]. However, these detectors suffer from significant losses, decreasing the device responsivity and requiring a specific technological process scheme for Ge [190].

To reduce the capacitance and increase the speed and responsivity, Ge waveguide photodetectors without Ge doping and top metal via-contacts like the Ge wrap-around configuration have been demonstrated [190, 191, 192, 193, 194, 195, 196, 197]. These devices show improved performance e.g. bandwidth, responsivity, dark current at the telecom and datacom wavelengths.

1.3.2.3 Switches

An optical switch can be used in many applications, like add/drop multiplexing, high-radix switch fabric. One type of optical switches is based on the plasma-dispersion effect [198, 199, 200], which has very fast switching speed (in nanoseconds). The other type is based on the thermo-optic effect [201, 202, 203, 204], thanks to the large thermo-optic (TO) coefficient of silicon. Although the TO-based switches have low loss, the switching speed is relatively slow (in microseconds). Ring-resonator based devices have a smaller footprint, but relatively narrower bandwidth, while Mach-Zehnder interferometer (MZI) based devices have a large footprint but much larger bandwidth.

1.4 Key Challenges for Silicon Photonic Transceivers

1.4.1 Maturity of Available Processes

Thus far, none of the commercially available silicon photonic processes are being offered to the public with yield and reliability guarantees. Furthermore, while these processes do come with a library of devices, these devices are often not at the state of the art in performance, and critical second-order parameters (e.g. linearity, back-reflection, performance across temperature, etc.) are not characterized. For photonic PDK's to be truly useful for commercial purposes, the depth of the device libraries and characterization data needs to be dramatically improved, and the models provided need to be supported with strong guarantees from the foundries.

1.4.2 Optoelectronic Design Flows

While significant work had been done on integrating optical primitives and simulation capabilities into existing design environments, the photonic simulations supported by these packages are relatively unsophisticated. As a result, the leaders in the silicon photonics space have been forced to develop their own device models, and often their own simulation software. While stand-alone photonic simulators are quite powerful for simulating both individual devices and systems-on-chip, there is not yet a commercial tool which is suitable for doing schematic design, simulation, layout, and test planning all within a single environment for chips composed of thousands to tens of thousands of elements. This is similar to the early days of the electronics industry, when leaders in the field were forced to develop their own design tools.

One particularly egregious omission is the lack of even an agreed-upon structure for describing the performance of individual photonic devices, in the same way that BSIM [205] provides models for the ASIC community. The silicon photonics community needs to work together to address these inadequacies, if we are to continue scaling complexity successfully. One of our goals as a community in the coming years should be to standardize on the shape of commercial-quality design flows, breaking these activities into a clear set of discrete steps, which the major EDA companies can address piece by piece.

1.4.3 Design for Packaging

One of the key challenges for silicon photonics is in moving complexity away from the package and into the chip, to reduce cost, because the product cost is typically dominated by the packaging. The electronics industry has a fully developed path for new chips to be post-processed (e.g. bumping), singulated, and attached to a substrate (e.g. pick and place, reflow, etc.). The photonics community has no comparable standard flow. While silicon photonics platforms have begun appearing at commercial foundries, photonic packaging is developed as a custom activity by each company developing a product line.

The key features of a silicon photonics package include the substrate attach, fiber attach and laser attach. While electronics chips are often bumped, and flip chipped, silicon photonics chips with pad counts in the low hundreds can use standard wire bonding or bumping technology, depending on the need. There are a few different coupling strategies in commercial use including grating couplers [25], active alignment [206] and v-grooves [207]. Laser attach techniques include heterogeneous integration of III-V on silicon [208], and laser chip bonding to the silicon photonics [209].

Considerable work [75] is currently ongoing to eliminate the need for hermeticity in packaging silicon photonic devices, and it's reasonable to expect that high-volume applications will in fact require non-hermetic packaging. Furthermore, it is reasonable to expect that as silicon photonics ramps into significant volume, some of the commercial package designs will either enter into the public domain or become available as commodity parts, at low cost.

1.4.4 Device Testing and Yield

In the electronics community, multiple vendors offer extremely mature probing solutions, suitable for a range of needs from early research through production. Automated equipment is extremely mature for die-by-die testing, the state of the art with regards to photonic probing of silicon wafers is considerably weaker. Most of the work in putting up wafer-scale test systems is not in the mechanical attachment of the fibers, which is relatively straightforward. The majority of the effort goes into developing test methodology for measuring devices quickly, at wafer scale, with very tight error bounds. In the silicon electronics space, special-purpose systems are offered with fully integrated

test equipment and well-understood recipes for standard tests. No comparable prober or set of test recipes is available for silicon photonics, and this represents an unfilled market niche.

1.4.5 Light Source

While considerable work has been done, both in the commercial and the academic spheres, on the development of light sources for silicon photonics [49, 210, 211, 212, 213], to our knowledge none of these processes are publicly available in the form of an MPW or a process with a commercial PDK. Silicon photonic chips are useless without a light source, whether it is on- or off-chip, and the development of on-chip or bonded light sources requires a very considerable effort. As the device count on-chip increases, the desirability of having light sources (lasers or amplifiers) on-chip only becomes greater, even if the insertion loss of the individual silicon photonic components continues to drop due to improved design and process innovation. As of now, there does not appear to be any prospect of a commercial-grade process which includes pre-designed, proven light sources becoming openly available in the immediate future.

1.5 Scope of Thesis

This thesis summarizes my research in silicon photonics, which spans from device design and optimization, to transceiver design and characterization, to applications of reconfigurable optical links in computing systems. The primary problems the thesis addresses are as follows:

- How to implement high-performance polarization/phase diversity devices in a silicon-on-insulator platform.
- How to implement high-speed silicon photonic transceivers in a silicon-on-insulator platform.
- How to improve the performance of multi-core many-memory computing systems using silicon photonic interconnects.

Chapter 2 and Chapter 3 present two different types of silicon photonic devices for polarization-diversity and phase-diversity communications, respectively. The demonstrated polarization rotators and 90° optical hybrids are key building blocks for advanced optical transceivers. Specifically, a novel device design and optimization methodology - particle swarm optimization in conjunction with 3D finite-time finite-division (FDTD), has been proposed and proved to be an effective way to design a wide range of passive silicon photonic devices.

Chapter 4 and Chapter 5 focuses on the design and characterization of the next-generation silicon photonic transceivers. For example, we demonstrate a polarization-insensitive WDM receiver with an aggregate data rate of 160 Gb/s. This receiver adopts a novel architecture which effectively reduces the polarization-dependent loss to less than 1.2 dB.

Chapter 6 focuses on chip-scale optical interconnects and presents two different types of reconfigurable memory interconnect for multi-core many-memory computing systems. These reconfigurable interconnects can effectively alleviate the memory access issues, such as non-uniform memory access, and NoC hot-spots that plague the many-memory computing systems by dynamically directing the available memory bandwidth to the required memory interface.

Chapter 7 summarizes the major results of the thesis and discusses the future work arising from the studies.

Part I

Passive Devices

Chapter 2

Polarization Rotator for Polarization-Diversified Circuits

This chapter reviews the author's work on designing and testing polarization rotators on a 220-nm silicon-on-insulator (SOI) platform.

Notable contributions of this work:

- Demonstration of a novel passive device design methodology by using particle swarm optimization and 3D FDTD simulation.
- The design methodology is easily extensible to other wavelength bands, like O-band or L-band.
- The rotator has a measured polarization conversion loss lower than 0.2 dB and a polarization extinction ratio larger than 25 dB over a wavelength range of 80 nm around 1550 nm.

2.1 Topology Optimization of Passive Silicon Photonic Devices

The design of passive silicon photonic devices in most cases can be summarized as a topology optimization problem, because the materials are relatively simple, and the geometric dimensions matter more. There are mainly three categories of topology optimization methodologies, as summarized in Table. 2.1.

Methodology	**Conventional**	**Evolutionary-Computation**	**Inverse Design**
Type	Manual	Automated	Automated
Method or Algorithm	Analytical Calculation/Brute Force	Particle Swarm/Genetic	Steepest-descent/Direct-Binary-Search
Design Space/Number of Parameters	2 - 5	20 - 50	200 - 500
Structure Granularity	Large	Medium	Small
Total Design/Computing Time	Several Days/Weeks	Several Hours	Several Days
Computational Complexity/Hardware Requirement	Low	Moderate	High
Device Performance	Moderate	High	Moderate

Table 2.1: Comparison of different topology optimization methods.

The conventional design methodology can handle very basic silicon photonic devices, such as directional couplers [110], multimode interference couplers [214], grating couplers [215], and distributed Bragg reflectors [216]. In all these case, the design space is very small and only a few geometric parameters such as the height, width, gap, periodicity of the structures need to be optimized. The photonic designer can either calculate the geometric parameters using analytical formulas or compute the electromagnetic field response using numerical simulations such as finite element method (FEM), finite difference time domain (FDTD) method, or beam propagation method (BPM). A three-dimensional (3D) structures can be replaced by its two-dimensional analogy using the effective index method (EIM) [217] to speed up the simulation. This brute force approach is repeated until satisfactory performance is obtained. Usually, this trial-and-error method takes long time, and does not exploit the full potential of the device geometry.

To search through a much larger parameter space and design more complicated silicon photonic devices, an evolutionary-computation methodology such as genetic algorithms [101, 161, 218] and particle swarm optimization [160, 219, 220, 221] have been explored. These methods rely on the evolutionary algorithm to quickly search a large design space and provide near-optimum designs. This method has proven to be very effective and efficient in designing a myriad of devices.

Recently, the inverse design methodology, which computes the local gradient of a

performance metric using steepest-descent optimization has attracted a lot of attention. The inverse design method allows for design by specification, whereby the silicon photonic designer simply specifies the desired functionality of the device, and the algorithm finds a structure which meets these requirements [222, 223, 224]. Although the inverse design method can deal with the largest number of parameters among the three methods and some designs are truly novel and counter-intuitive, the designs usually suffer from high fabrication sensitivity [225, 226, 227, 228].

2.2 Polarization Rotator

A polarization rotator (PR) or polarization splitter-rotator (PSR) is a crucial component for implementing polarization-transparent circuits [229] and polarization-diversity circuits [230, 231]. The losses of PSRs are usually much smaller than the use of two-dimensional grating couplers [144, 232, 233] to achieve polarization diversity. Recently, the implementations of on-chip PRs, especially in a silicon-on-insulator (SOI) platform, have received much attention [234, 235, 236, 237, 237, 238, 239, 240]. Among these, PRs that can be fabricated with a complementary metal oxide semiconductor (CMOS) compatible process are particularly attractive.

Mode-evolution-based PRs are a family of rotators that are widely used in today's polarization-diversified circuits. Chen et al. [236] demonstrated a high-efficiency PR with a device length of 420 μm using an additional S_3N_4 structure located on top of a silicon waveguide. Sacher et al. [237] recently presented an adiabatic bi-level taper polarization rotator-splitter (PRS) with a device length of 475 μm. Although CMOS-compatible PRs with a symmetric SiO_2 cladding can be achieved, as shown by the aforementioned demonstrations, the footprints of these devices are still very large. Recently, polarization rotators based on surface plasmon polaritons (SPPs) have been widely explored in the literature [241, 242]. Although the polarization conversion lengths of these SPP-based PRs are smaller, the insertion losses (ILs) of these devices are quite high ($\sim$2 dB). Fabrication barriers must also be overcome to make SPP PRs fully compatible with the CMOS process. Therefore for PRs, a legitimate question, is then: Can a PR be realized with both small footprint and high conversion efficiency, while at the same time being CMOS-compatible and tolerant of manufacturing?

2.3 Design and Optimization

2.3.1 Device Design

We present a CMOS-compatible PR with both a small footprint and high conversion efficiency. As shown in Fig. 2.1, our proposed PR comprises an ultra-short bi-level TM0-to-TE1 mode converter, and a novel TE1-to-TE0 mode converter, both of which are realized on the SOI platform with a symmetric SiO_2 cladding. The blue regions represent the full height of the Si (220 nm thick), while the yellow regions represent the partially-etched Si slab (90 nm thick). Notice that the PR transforms from a narrow strip waveguide (at the input), to ridge waveguides (along the bilevel taper), and finally to a wide strip waveguide (along the bent taper). The proposed PR is based on the higher-order-mode-assisted mode rotation principle. Instead of rotating the mode directly, the higher-order-mode-assisted PRs use a higher order mode (usually a second-order mode, e.g. the TE1 or TM1 mode) as a transition between the two orthogonal modes (the TE0 and TM0 modes). As shown in Fig. 2.1, the input TM0 mode is first launched into the right-hand side of this PR. It then gradually changes into the TE1 mode when passing through the bi-level taper. Subsequently, the TE1 mode will be converted into the TE0 mode with the assistance of the bent taper. Also note that in Fig. 2.1 - Fig. 2.4 the longitudinal scale is compressed with respect to the cross-sectional scale to simplify viewing.

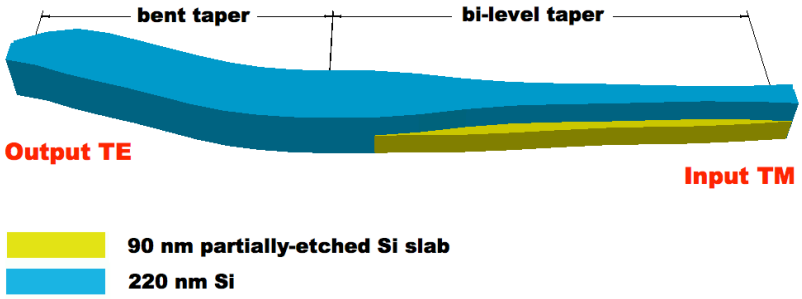


Figure 2.1: Schematic of the PR, consisting of a bi-level taper and a bent taper. The PR is surrounded by a symmetric SiO_2 cladding (a buried oxide bottom-cladding and a SiO_2 top-cladding).

The design goal is to find the optimum geometric parameters of the proposed PR

that can achieve a high polarization conversion efficiency (PCE) with the most compact footprint. To meet this goal, we chose the particle swarm optimization (PSO) method, which has been shown to be an effective technique in designing compact and high-performance passive devices [160, 219].

The design of a bi-level TM0-to-TE1 mode converter had been discussed and experimentally demonstrated in literature [237, 238, 243, 244]. The mode conversion can be almost lossless in such a linear bi-level taper architecture. However, mode conversion in such linear adiabatic tapers is not efficient. The length of the linear adiabatic taper is usually around a hundred microns or even longer in order to achieve high conversion efficiency ($> 95\%$) [237, 238]. On the other hand, if the taper geometry is carefully engineered to be nonlinear, one can expect significant improvement of the mode conversion efficiency and a reduction in the footprint of the PR.

2.3.2 Device Optimization

We now elaborate the use of the PSO method to design an ultra-efficient bi-level mode converter. As shown in Fig. 2.2(a), the thicknesses of the ridge level (colored in blue) and the partially-etched slab level (colored in yellow) are 220 nm and 90 nm, respectively. The taper is symmetric and digitalized to 10 segments with interpolations between one another, similar to the published PSO technique [160]. The length of this bi-level converter is only 9 μm, which is an order of magnitude smaller than any other previously published devices. The field pattern of this taper is shown in Fig. 2.2(b). TM0 mode is launched into the left side, and it quickly converts to a TE1 mode with minimum scattering loss. Notice that the first 1 μm at the left is a 500 nm wide strip waveguide, where the mode is launched. As shown in Fig. 2.2(c), PCE higher than 97% is achieved across an 80 nm wavelength range around 1550 nm. This is calculated using Lumerical three-dimensional finite-difference time-domain (3D FDTD) software. The refractive indices of Si and SiO_2 at 1550 nm are 3.476 and 1.445, respectively. The dispersions of Si and SiO_2 have been considered in the simulation. The widths of the ridge waveguide and partially-etched slab are listed in Table. 2.2.

Next, we will discuss the design of a novel TE1-to-TE0 mode converter. Different TE1-to-TE0 conversion schemes have been proposed in the literature using different devices such as a directional coupler (DC) [245, 246], a multimode interference

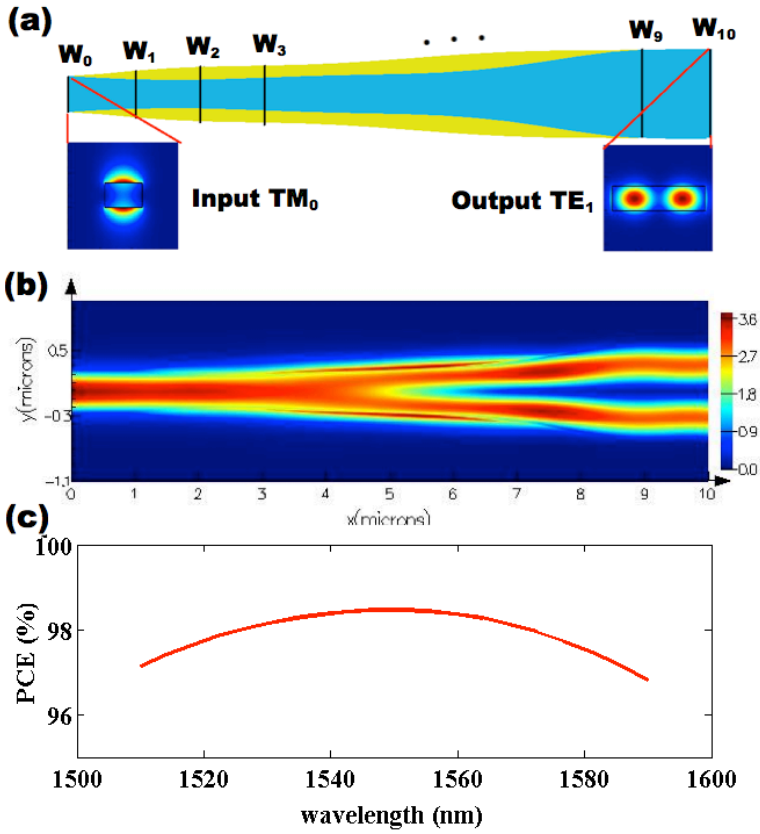


Figure 2.2: (a) Schematic of the bi-level taper (top view). The taper geometry is defined by spline interpolation of W0 to W10. (b) Simulated power distribution at 1550 nm wavelength. (c) Simulated PCE.

(MMI) coupler [247], a microring [248], and an asymmetric Mach-Zehnder Interferometer (MZI) [238, 249]. However, each scheme has its limitations. For example, the DC-based mode conversion scheme has an intrinsic bandwidth limitation, while the MZI-based mode conversion scheme is sensitive to fabrication deviations as it depends on the exact phase-delay between arms.

Here, we demonstrate for the first time a wideband, compact and high-efficiency TE1-to-TE0 mode converter based on a single layer S-bend-like waveguide structure, which we refer to as a bent taper. After optimizing the geometry with PSO, almost perfect mode conversion efficiency can be achieved within a very short working distance. Schematic of the proposed design is shown in Fig. 2.3(a). In general, an S-bend waveguide can be defined by three parameters: radius R0 of the arc of the center of the

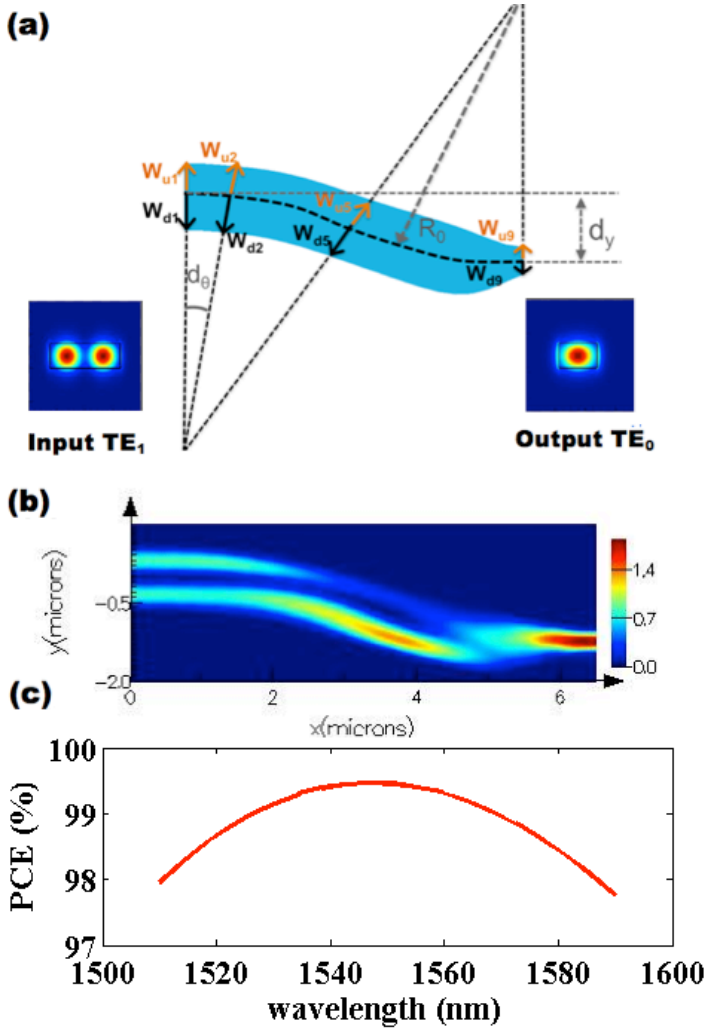


Figure 2.3: (a) Schematic of the bent-taper TE1-to-TE0 mode converter (top view). (b) Simulated power distribution at 1550 nm wavelength. (c) Simulated PCE.

waveguide, vertical offset dy, and waveguide width W. Do note that W is a constant for a normal S-bend. One often avoids routing with a wide S-bend to avoid multimode interference. However, such multimode interference can be very desirable if one can

Layer	W0	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10
Ridge	500	413	401	457	518	554	624	807	1077	1248	1250
Slab	500	648	759	795	848	960	1096	1191	1225	1237	1250

Table 2.2: Taper width in nm.

control its behavior. The behavior of the S-bend can be controlled by engineering its geometry. Instead of fixing the width W as a constant, W is varied at different angles in this work. We also discretized the S-bend into 9 segments of equal angles, dθ, followed by interpolation between each segment. This will make the transition of geometry smooth. Instead of defining a symmetric S-bend (now relative to the center radius R0) as in TM0-to-TE1 taper, we now choose an asymmetric geometry for the S-bend to increase the optimization freedom. The center radius R0 divides the S-bend into two sides: the up side and the down side. Therefore, we have two sets of independent width parameters: Wu1, Wu2, Wu3, ..., Wu9 and Wd1, Wd2, Wd3, ..., Wd9 , as indicated in Fig. 2.3(a).

The TE1 mode is launched in at the wide end (left of Fig. 2.3(a)), which has a waveguide width of 1.25 μm and the TE0 mode emerges at the narrow end (right of Fig. 2.3(a)), which has a width of 0.5 μm. Note that the 1.25 μm wide end is chosen to match the above optimized TM0-to-TE1 mode convertor, while the 0.5 μm narrow end is the standard width of the single mode waveguide for waveguide routing.

During optimization, we fixed the vertical offset dy to be 1.2 μm, and optimized the center radius R0 as well as the waveguide width sets. We found that lossless conversion (99.5% efficiency, Fig. 2.3(c)) can be achieved by only optimizing the center radius and the last two segments (Wu7, Wu8, Wd7, Wd8). The width of the first 6 segments was kept the same as the wide end, which has a width of 1.25 μm. R0 is found to be 8.531 μm after optimization. The length of the bent taper is calculated to be 6.3 μm. The detailed geometric parameters are provided in Table. 2.3.

Generally speaking, the TE1 mode can be effectively regarded as combination of two anti-phase TE0 modes. The phase mismatch must be overcome to convert the TE1 mode into the TE0 mode. As seen in Fig. 2.3(b), this simple and ultra-compact design allows the two anti-phase components of TE1 mode to travel with different effective lengths and adiabatically combine into the TE0 mode at the narrow end. Meanwhile,

Wu1	**Wu2**	**Wu3**	**Wu4**	**Wu5**	**Wu6**	**Wu7**	**Wu8**	**Wu9**
625	625	625	625	625	625	616	426	250
Wd1	**Wd2**	**Wd3**	**Wd4**	**Wd5**	**Wd6**	**Wd7**	**Wd8**	**Wd9**
625	625	625	625	625	625	695	635	250

Table 2.3: Converter width in nm.

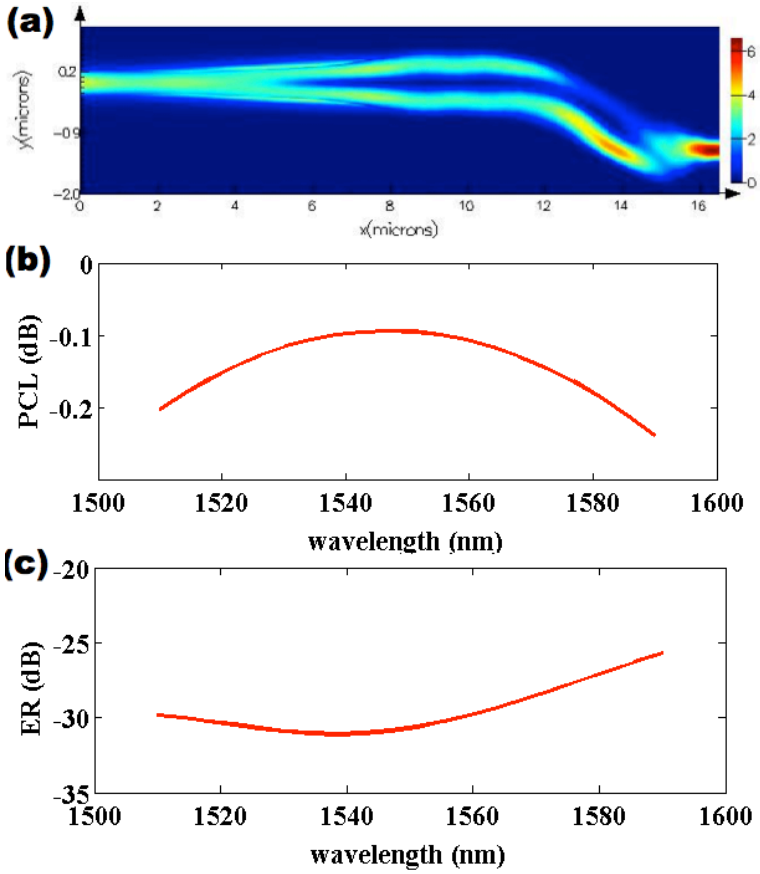


Figure 2.4: (a) Simulated power distribution at 1550 nm wavelength. The input TM0 mode is launched from the left port, and the TE0 mode comes out from the right port. (b) Simulated polarization conversion loss (PCL). (c) Simulated extinction ratio (ER) of the entire PR.

since the mode conversion happens within a single waveguide, broadband performance is automatically achieved.

Finally, we combined the two converters discussed above to form the complete TM0-to-TE0 PR. The behavior of this device was verified with 3-D FDTD simulation. Fig. 2.4(a) shows the mode profile when launching TM0 mode at the left port. Fig. 2.4(b) and Fig. 2.4(c) show the total polarization conversion loss and the extinction ratio of the proposed PR, respectively. As shown in Fig. 2.4(b), the PR shows less than 0.2 dB polarization conversion loss over a bandwidth of 80 nm. The extinction ratio is larger than 25 dB over the same wavelength range. The PR achieves a maximum extinction ratio of 30 dB at 1550 nm.

2.3.3 Fabrication Tolerance Analysis

To investigate the fabrication tolerance, three key geometric parameters (the height of partially-etched slab, the width of un-etched ridge waveguide, and the width of partially-etched slab) have been varied within ±40 nm.

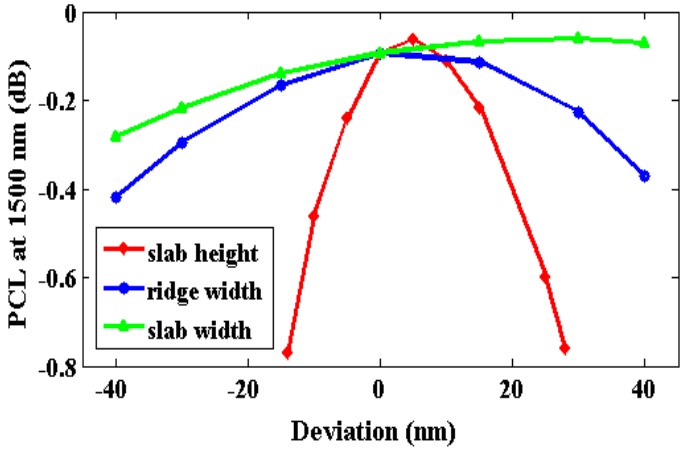


Figure 2.5: Simulated PCL at 1550 nm for the fabrication deviation on the abscissa in the height of the partially-etched slab (red), the width of the un-etched ridge waveguide (blue), and the width of the partially-etched slab (green).

As shown in Fig. 2.5, the polarization conversion loss does not experience any serious degradation as the width of the un-etched ridge waveguide or the width of the partially-etched slab change. Thus, it is safe to conclude that the device has a high fabrication tolerance towards even ±40 nm width deviations. It is also evident that this device is relatively sensitive to the height of the partially-etched slab. But if we can control the height deviation of the partially-etched slab within ±10 nm (the actual height of the partially-etched slab ranges from 80 nm to 100 nm), the polarization conversion loss of the PR will not exceed 0.5 dB, which is quite decent. Overall, this device is fabrication insensitive and could be fabricated using optical lithography.

The temperature dependence of Si has been measured to be $\frac{\partial n}{\partial T} = 1.87 \times 10^{-4} K^{-1}$ at 1500 nm [250]. The temperature dependence of SiO_2 is 6× lower than Si [251]. Based on 3D FDTD simulation results, temperature-induced refractive index changes do not cause a significant wavelength shift of the proposed polarization rotator.

2.4 Fabrication and Measurement

2.4.1 Device Fabrication

The polarization rotator is fabricated using a CMOS-compatible process flow, as shown in Fig. 2.6. It starts from a 220 nm SOI wafer with a 2.5 μm BOX. A hard mask layer is deposited on the top silicon layer. Then, using a partial etch step to remove 115 nm of Si creates the strip-loaded layer, followed by a full etch step to form the ridge waveguide. After that, the hard mask is removed, and oxide is deposited to cover the waveguides.

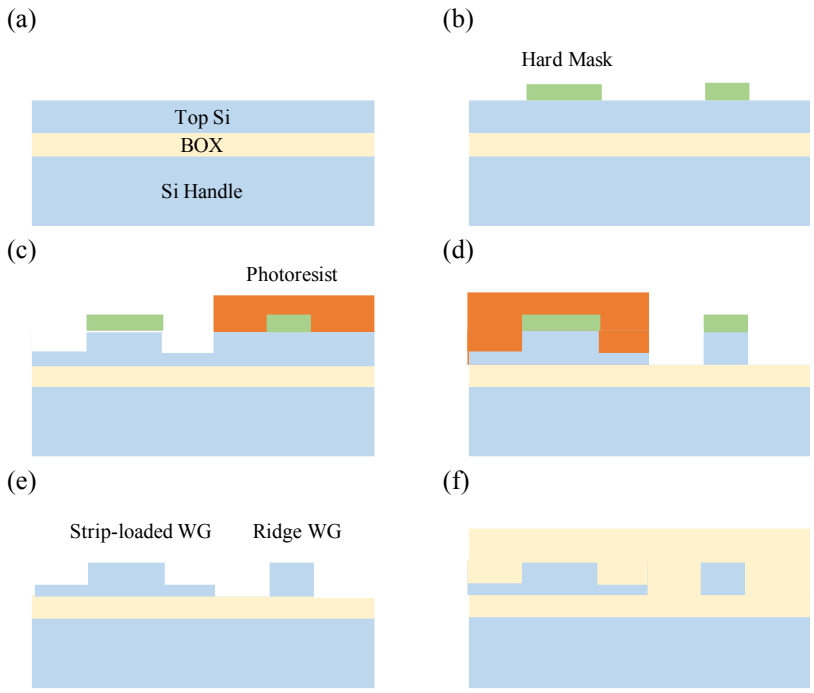


Figure 2.6: Process flow (a) initial 220 nm-thick top silicon SOI wafer, (b) define hard mask, (c) partial etch to create strip-loaded waveguide, (d) full etch to create ridge waveguide, (e) hard mask removal, and (f) oxide deposition.

Fig. 2.7 shows the fabricated rotator. Note the rotator shown in the image uses a longer bilevel taper. As stated above, the longitudinal scale in Fig. 2.1 - Fig. 2.4 is compressed with respect to the cross-sectional scale, but Fig 2.7 is a photo-micrograph with a uniform scale in all directions.

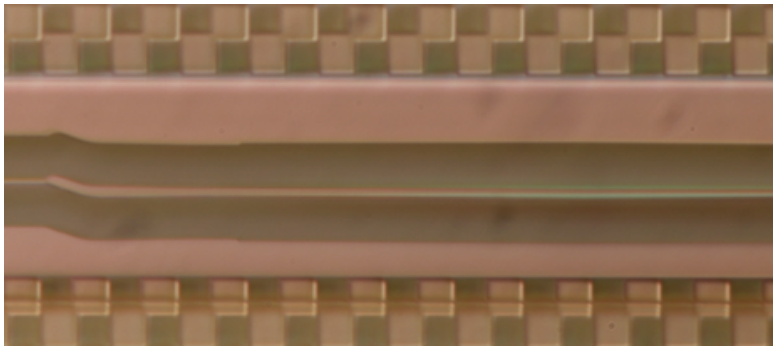


Figure 2.7: Optical image of the fabricated polarization rotator.

2.4.2 Device Measurement

The device performance was characterized on a wafer-scale optical test setup, by means of grating couplers. Fig. 2.8 and Fig. 2.9 show parameters measured on one wafer and across different wafers, respectively. The optical parameters, polarization conversion loss (∼0.1 dB) and polarization extinction ratio (∼20 dB) show good performance was achieved.

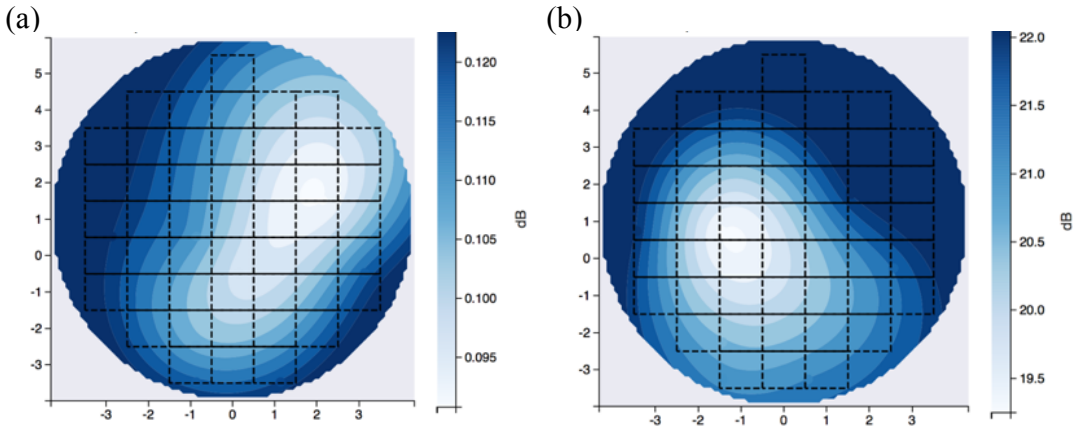


Figure 2.8: (a) Contour plot of the measured polarization conversion loss in one wafer (b) Contour plot of the measured polarization extinction ratio in one wafer.

2.5 Discussion

The demonstrated polarization rotator has four advantages: (1) ultra-low loss, (2) use of only silicon without any extra auxiliary materials, (3) compact footprint, and (4)

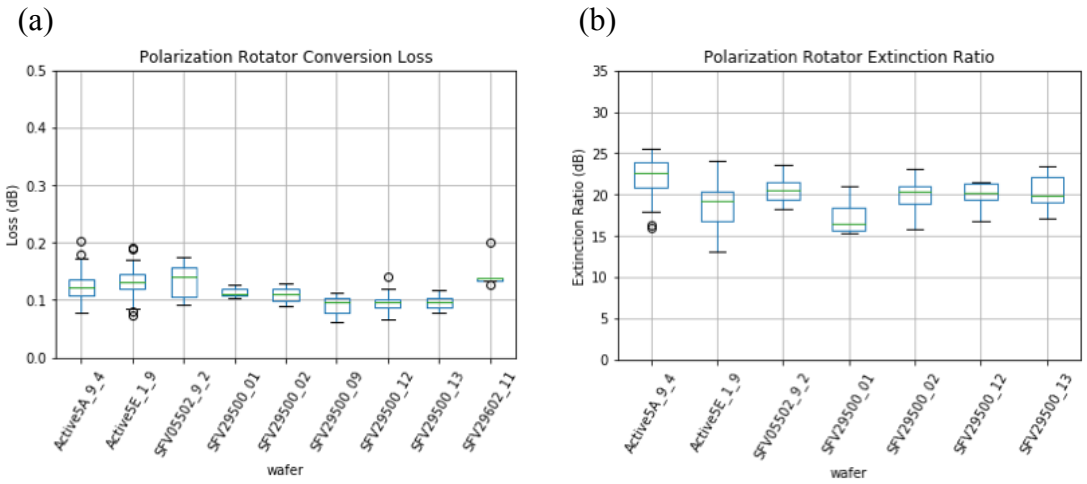


Figure 2.9: (a) Measured polarization conversion loss across different wafers. (b) Measured polarization extinction ratio across different wafers.

robust against manufacturing variation. Table. 2.4 compares the performance of our device with other published polarization rotators. Our work shows the lowest measured polarization conversion loss. The measured bandwidth and polarization extinction are also excellent.

Reference	**[236]**	**[252]**	**[237]**	**[253]**	**[226]**	**This Work**
Publication Date	2011	2013	2014	2015	2017	2014
Material	SOI/S_3N_4	SOI/Silver	SOI	SOI	SOI	SOI
Type	Mode Evolution	Plasmonic	Mode Evolution Double-Layer	Double-Stair	Digital Metamaterial	PSO-Optimized Bilevel
Footprint (μm × μm)	420x2 (840)	5x4 (20)	450x10 (4500)	23x2 (46)	8x1.5 (12)	15x4 (60)
Bandwidth (nm)	60	90	50	17	40	60
Conversion Loss (dB)	1.5	2.1	1.5	2.5	4.3	0.2
Extinction Ratio (dB)	30	14	13	40	9	25

Table 2.4: Performance comparison of recent polarization rotator works.

2.6 Conclusion

In conclusion, we have designed an ultra-compact and high-efficiency PR using a bi-level-tapered TM0-to-TE1 mode converter and a novel TE1-to-TE0 mode converter. PSO is used to optimize the geometric parameters. The device has a length of 15.3 μm and shows a simulated insertion loss better than 0.2 dB over a bandwidth of 80 nm. Fabrication of our proposed PR is CMOS-compatible using pure silicon with a SiO_2 top-cladding, without any extra auxiliary layers like S_3N_4.

Chapter 3

Optical Hybrid for Coherent Communication

The work in this chapter is about a compact and low-loss 90° optical hybrid on a silicon-on-insulator (SOI) platform for coherent receivers. Our 90° optical hybrid uses a novel topology, comprising one Y-junction and three 2×2 multimode interference (MMI) couplers. The geometry of the 90° optical hybrid is fully optimized using particle swarm optimization (PSO). The fabricated 90° optical hybrid has a compact footprint of 21.6 μm × 27.9 μm, with an insertion loss less than 0.5 dB, a common mode rejection ratio (CMRR) larger than 30 dB, and phase error smaller than 3° over the C-band and across 22 reticles on one wafer. The measured phase error ($< 3°$) in a packaged coherent receiver further confirms the excellent performance of the 90° optical hybrid.

Notable contributions of this work:

- Demonstration of a novel 90° optical hybrid topology.
- First study of optical hybrid to the overall coherent transceiver performance.
- Demonstration of 90° optical hybrid with the most compact footprint and the smallest phase error compared to the previously published devices.

3.1 Optical Hybrid

The rapid growth of long distance data transmission demand has driven the development of optical transmission systems with high spectral efficiency, high channel data

rate, and low cost [3, 254]. To economically extend the reach and data capacity of next-generation networks, coherent optical communication technologies using modulation formats like quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM) have been widely deployed in long-haul networks [78, 255]. Compared to traditional transmission systems, coherent optical transmission systems offer better spectral efficiency and receiver sensitivity as well as better tolerance to amplified spontaneous emission (ASE) noise, chromatic dispersion, and polarization mode dispersion (PMD) [256]. In addition to their use in long-haul networks, coherent transmission technologies are also being used in metro networks where traffic loads require use of transceivers on a much larger scale [257, 258].

A 90° optical hybrid is a key component in coherent transmission systems. It mixes the incoming received signal with the reference signal (local oscillator or LO) and delivers four light signals to two pairs of balanced detectors. Those signals can then be mapped to four complex-field space signals: modulation in-phase with the reference carrier and in-quadrature-phase to the reference, each on two orthogonal states of polarization. There are two major types of 90° optical hybrids: Type-I is based on several discrete components such as 1×2 couplers, 2×2 couplers and phase shifters [259, 260, 261, 262]; Type-II is based on a single device such as a 4×4 multimode interference (MMI) coupler [263, 264]. There are designs constructed by 2×4 MMI couplers followed by 2×2 MMI couplers [265, 266, 267], which can be regarded as a derivative of Type-II hybrid.

Type-I hybrids have been demonstrated in silica-based planar lightwave circuits [260, 268] and LiNbO3-based integrated circuits [269]. Recently, Type-I hybrids which avert waveguide crossings to mitigate crosstalk have been demonstrated on a silicon-on-insulator (SOI) platform [261, 262]. These designs require accurate control of phase in the waveguides [270], a feature which is difficult to achieve in high-index-contrast photonics platforms due to waveguide sidewall roughness and thickness variations. Thermal phase shifters can be implemented to tune the phase to the desired value [259], but this design creates complexities for control of real systems.

Type-II hybrids are generally the solution of choice in high-index-contrast platforms like deeply-etched indium phosphide (InP) [264, 265, 271] and silicon-on-insulator [263, 266, 272] because they are fully passive and require no active control loop to stabilize the 90° phase relation. However, governed by the self-imaging theory [107, 214, 273], to

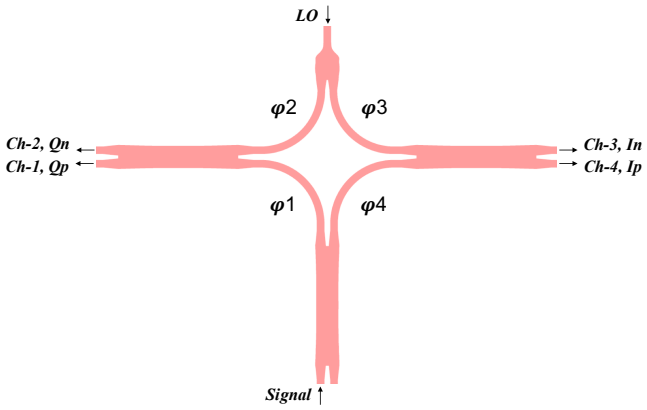


Figure 3.1: Schematic diagram of the proposed 90° optical hybrid.

realize optimum self-imaging, 90° optical hybrids based on 4×4 MMI couplers or 2×4 MMI couplers usually have a length of hundreds of micrometers. This requirement not only hinders the further scaling-down of the footprint, but more importantly it results in low-quality imaging because of the strong phase errors of the higher-order modes [272]. Due to mode dispersion, it is difficult for Type-II hybrids to achieve broadband self-imaging. Therefore, loss and phase error in Type-II hybrids exhibit strong wavelength dependence and process dependence. For commercial purposes, the critical parameter is usually not the performance at the best wavelength, but performance at the worst wavelength, therefore making it very challenging to meet the tight requirements for high-order QAM.

3.2 Design and Optimization

3.2.1 Device Design

Fig. 3.1 shows the schematic diagram of the proposed 90° optical hybrid which consists of one Y-junction and three 2×2 MMI couplers connected by four identical 90° bends. The signal and local oscillator (LO) inputs come through the bottom 2×2 MMI coupler and the top Y-junction, respectively. The quadrature channels (Q) are the outputs of left 2×2 MMI couplers, and the in-phase channels (I) are the outputs of the right 2×2 MMI couplers. Note that 2×2 MMI couplers in the schematic diagram can be replaced with other types of 2×2 couplers like 3-dB directional couplers.

The quadrature phase behavior of the 90° optical hybrid can be analytically described as follows: If we set the electric field of the signal (ES) and the LO (ELO) to be the input of the bottom 2×2 MMI coupler and the input of the Y-junction, then the output fields of the 90° optical hybrid are represented by

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \end{bmatrix} = \big[T_3\big] \cdot \big[T_2\big] \cdot \big[T_1\big] \cdot \begin{bmatrix} E_S \\ E_{LO} \\ 0 \\ 0 \end{bmatrix} \tag{3.1}$$

In Eq. 3.1, [T1] indicates the transfer matrix for the Y-junction and the bottom 2×2 MMI coupler. [T2] is the transfer matrix for the four 90° bends, and [T3] is the transfer matrix of the left and right 2×2 MMI couplers.

$$\big[T_1\big] = \sqrt{\kappa} \cdot \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ e^{j\theta} & 0 & 0 & 0 \end{bmatrix} \tag{3.2}$$

$$\big[T_2\big] = \begin{bmatrix} e^{j\varphi_1} & 0 & 0 & 0 \\ 0 & e^{j\varphi_2} & 0 & 0 \\ 0 & 0 & e^{j\varphi_3} & 0 \\ 0 & 0 & 0 & e^{j\varphi_4} \end{bmatrix} \tag{3.3}$$

$$\big[T_3\big] = \sqrt{\kappa} \cdot \begin{bmatrix} 1 & e^{j\theta} & 0 & 0 \\ e^{j\theta} & 1 & 0 & 0 \\ 0 & 0 & 1 & e^{j\theta} \\ 0 & 0 & e^{j\theta} & 1 \end{bmatrix} \tag{3.4}$$

where κ indicates a power splitting coefficient of the 2×2 MMI coupler and θ is the phase shift introduced by the 2×2 MMI coupler. $\varphi 1$, $\varphi 2$, $\varphi 3$, and $\varphi 4$ are the phase shifts introduced by the four bends. By plugging Eq. 3.2 - Eq. 3.4 into Eq. 3.1, we have Eq. 3.5

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \end{bmatrix} = \kappa \cdot \begin{bmatrix} e^{j\varphi_1} E_S + e^{j(\theta+\varphi_2)} E_{LO} \\ e^{j(\theta+\varphi_1)} E_S + e^{j\varphi_2} E_{LO} \\ e^{j(2\theta+\varphi_4)} E_S + e^{j\varphi_3} E_{LO} \\ e^{j(\theta+\varphi_4)} E_S + e^{j(\theta+\varphi_3)} E_{LO} \end{bmatrix} \tag{3.5}$$

We now separate our discussion into two different cases - an ideal case and a realistic case. In the ideal case, we assume perfect phase shift of the 2×2 MMI couplers $\theta =$

$\pi/2$ and the phase shifts introduced by the 90° bends satisfy the condition given by Eq. 3.6

$$\varphi_1 = \varphi_4 \quad and \quad \varphi_2 = \varphi_3 \tag{3.6}$$

If we further consider perfect power balance ($\kappa = 1/2$) and ignore any constant phase offset, then Eq. 3.5 can be simplified to Eq. 3.7. Since the phase relation at the outputs is rotated by 90° relative to each other, the proposed scheme works as a 90° optical hybrid.

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} E_S + jE_{LO} \\ E_S - jE_{LO} \\ E_S - E_{LO} \\ E_S + E_{LO} \end{bmatrix} \tag{3.7}$$

In the realistic case, the assumptions above about the phase shifts of the 2×2 MMI couplers and the 90° bends do not hold because of variation in fabrication. Phase error of the proposed 90° optical hybrid is defined as the difference in phase from 90° in Eq. 3.8.

$$\frac{\pi}{2} - (\varphi_2 - \varphi_1) - (\varphi_4 - \varphi_3) - \theta \tag{3.8}$$

Phase error of the proposed 90° optical hybrid comes from two sources: 2×2 MMI coupler phase uncertainties and waveguide phase uncertainties. Phase variations in a high index contrast Si waveguide comes from all kinds of non-idealities in fabrication; to name a few: non-uniform waveguide width due to lithography, waveguide sidewall roughness, and SOI wafer thickness variation. The phase error of our 2×2 MMI coupler is within 1.2° based on the simulations as shown in Fig. 3.2(d). The phase error from the four 90° bends can be estimated using coherence length theory [274]. The coherence length of two uncorrelated waveguides was reported to be ∼4 mm in a silicon photonics platform with 248 nm lithography [275]. If we assume the total length in the curved waveguide routing is 25 μm (corresponding to ∼4 μm bend radius), the phase uncertainty would be 6.4°. This estimation defines a guideline for the design since phase coherence length strongly depends on the fabrication process and the distance between two waveguides [276]. Based on this analysis, we chose a 4 μm bend radius for the proposed 90° optical hybrid. As demonstrated in Section 3, the measured phase

error of the 90° optical hybrid is below 3° in the C-band, which is the best, to our knowledge, that has been reported so far.

3.2.2 Device Optimization

The goal is to find the optimum geometry for the proposed 90° optical hybrid that can achieve low insertion loss, low phase error, and high CMRR with a compact device footprint. To meet this goal, we adopt PSO which has been widely used in designing compact and high-performance passive devices [160, 219, 277].

The design of our 90° optical hybrid is a two-step process. In the first step, we design and optimize all three subcomponents, including the Y-junction, the 90° bend, and the 2×2 MMI couplers, individually. For the Y-junction, we use an improved design of our previous work [219] with excess loss < 0.1dB across the C-band. For the 90° bends, we use the normal 90° bends with bend radii of 4 μm. The typical loss of a small radius 90° bend is on the order of 0.01 dB [278], a sufficiently low loss for our application. Although ultralow loss 90° bends [279, 280] exist and are preferred for large-scale photonic integrated circuits, they are not necessary for this individual 90° optical hybrid.

A traditional 2×2 MMI coupler has a rectangular shape. Design freedom is thus limited to the width and the length of the MMI coupler. The traditional 2×2 MMI coupler suffers from high scattering loss at the input/output ports and high output power imbalance due to imperfect self-imaging. Here we introduce the design methodology of a compact, low-loss, and low-imbalance 2×2 MMI coupler by breaking the rectangular geometry constraint.

Fig. 3.2(a) illustrates a schematic diagram of the 2×2 MMI coupler, that is symmetric about both the x-axis and the y-axis. Four tapers provide adiabatic transitions between the interconnecting waveguide (W4) and the MMI access waveguides (W5) to further reduce mode-mismatching loss. W6 is the gap between two tapers with W3 equal to 2W5+W6. The multimode region is digitalized into 4 segments with interpolations between each segment. W1, W2, W3, L2, and L3 are optimized to yield the minimum imbalance and insertion loss. The optimization figure of merit (FOM) is:

$$\sum (0.5 - y_1(\lambda))^2 + (0.5 - y_2(\lambda))^2 + (y_1(\lambda) - y_2(\lambda))^2 \tag{3.9}$$

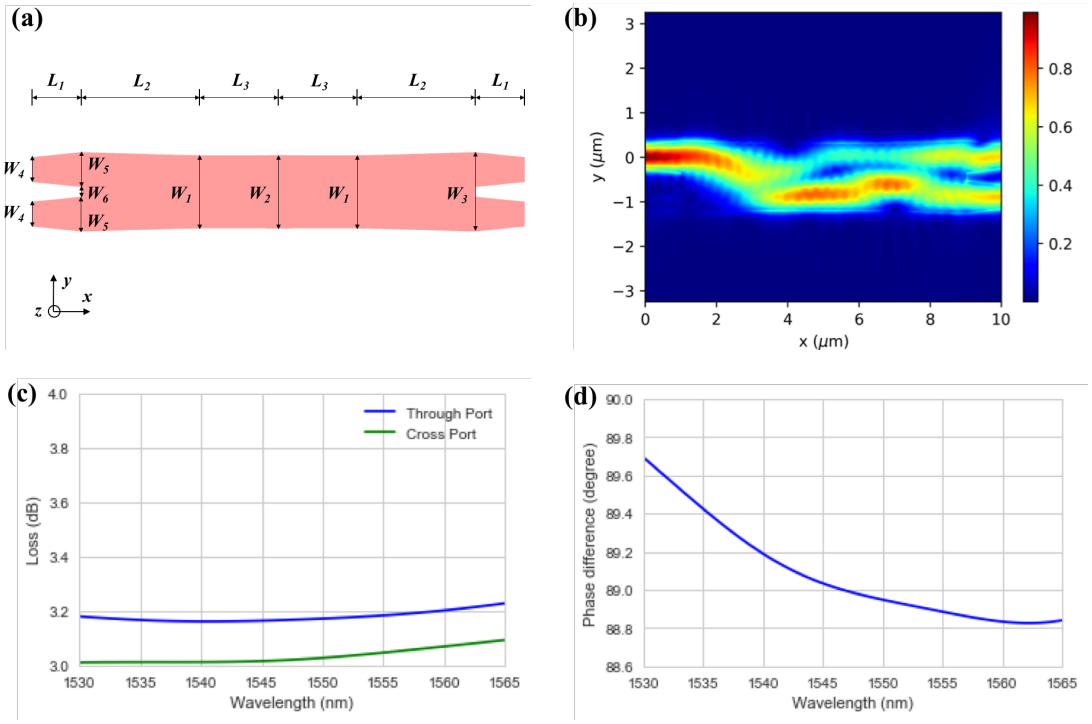


Figure 3.2: (a) Schematic of the 2×2 MMI coupler (top view). The 2×2 MMI geometry is defined by cubic interpolation of W1 to W3. (b) Simulated power distribution at 1550 nm wavelength. (c) Simulated 2×2 MMI coupler insertion loss. (d) Simulated 2×2 MMI coupler phase difference between the through port and the cross port.

where y1(λ) and y2(λ) correspond to the normalized optical power at the through and cross ports of the 2×2 MMI coupler, respectively. The PSO optimization was run in Lumerical's 3-D FDTD.

The resulting dimensions are listed in Table. 3.1. The top-view of the simulated electric field is shown in Fig. 3.2(b). Fig. 3.2(c) shows the insertion loss of the through port and cross port as a function of wavelength. Note that the intrinsic 3 dB loss for each port has not been deducted. Fig. 3.2(d) shows the phase error is less than 1.2° across the C-band.

W1	W2	W3	W4	W5	W6	L1	L2	L3
1.48	1.48	1.6	0.5	0.7	0.2	1	2.4	1.6

Table 3.1: 2×2 MMI geometric parameters in μm.

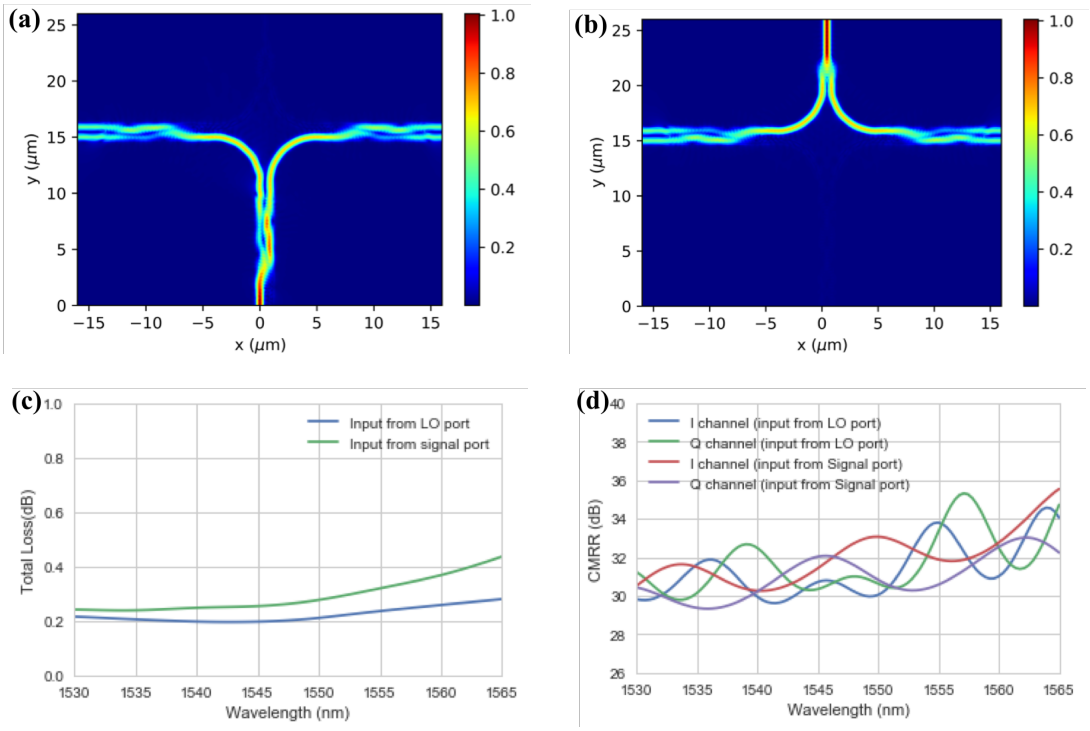


Figure 3.3: Simulated E-field distribution at 1550 nm wavelength (a) when input from the signal port, (b) when input from the LO port. (c) Simulated total insertion loss. (d) Simulated CMRR.

In the second step, with all the subcomponents ready, the design of the 90° optical hybrid is straightforward, that is to connect them together following the topology in Fig. 3.1. We verify the performance of the 90° optical hybrid using 3-D FDTD simulation. Fig. 3.3(a) and Fig. 3.3(b) are the top-views of mode propagation through the 90° optical hybrid with input from just the signal port or LO port, respectively. Fig. 3.3(c) shows the total insertion loss (the sum of losses from all four output ports) as a function of wavelength. The total insertion loss is less than 0.3 dB when input is from the LO port, and less than 0.45 dB when input is from the signal port. An excellent CMRR of 30 dB or better is achieved for both the LO port and signal port in the C-band.

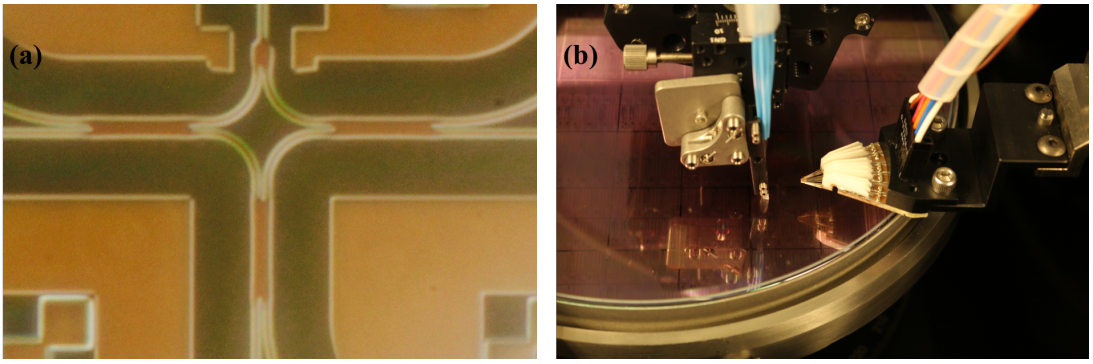


Figure 3.4: (a) Optical image of the fabricated 90° optical hybrid, and (b) Image of the automated wafer-level test setup.

3.3 Fabrication and Measurement

3.3.1 Device Fabrication

The device is fabricated in a 220-nm SOI platform [234]. Fig. 3.4(a) shows an optical image of the fabricated 90° optical hybrid. We implemented two kinds of test structures to characterize different performance metrics of the 90° optical hybrid. One kind of test structure has a Mach-Zehnder (MZ) delay interferometer with a length difference of 126 μm before the 90° optical hybrid used to extract phase error [265, 266]. The four outputs of the 90° optical hybrid are connected directly to grating couplers. The other kind of test structure has its LO and signal inputs connected directly to grating couplers, and its outputs are connected to photodetectors (PDs) to extract loss and CMRR.

3.3.2 Device Measurement

3.3.2.1 Across Wafer

The device is measured in an automated wafer-level test setup as shown in Fig. 3.4(b). Light from a tunable laser was coupled into the test structure via a polarization maintaining (PM) fiber array and grating couplers (GCs). Depending on the type of test structure, the outputs of the 90° optical hybrid came out either through the same PM fiber array and were measured using an optical power meter to extract the phase error or through a DC probe and were measured using source meters to extract loss and

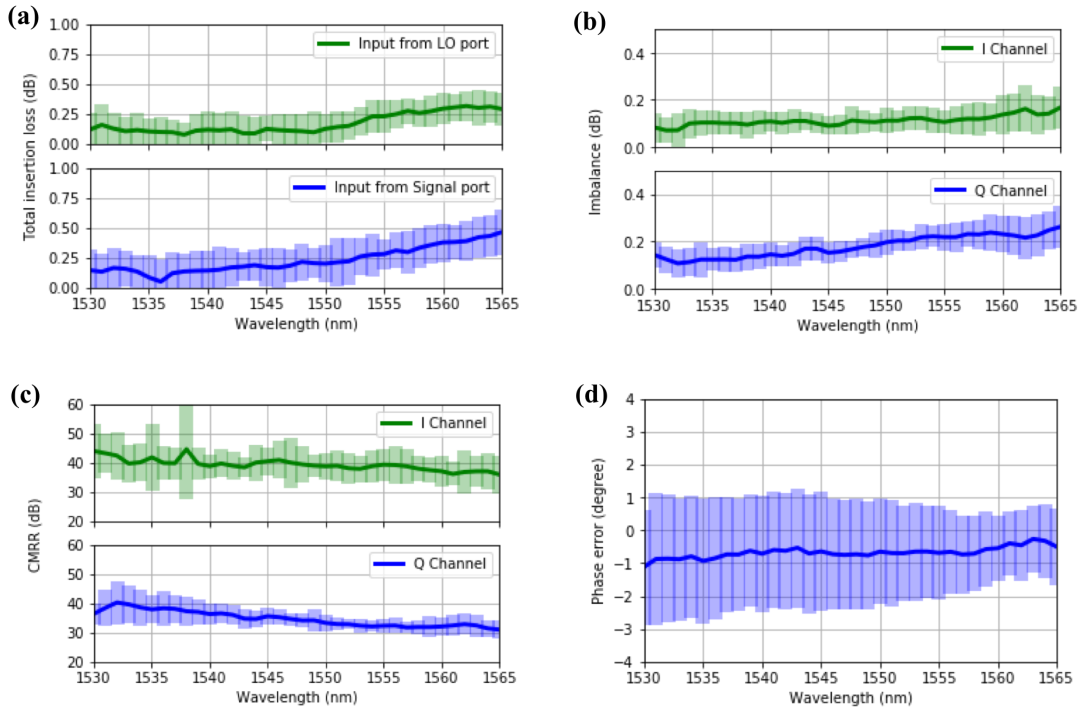


Figure 3.5: Measured (a) total insertion loss, (b) imbalance, (c) CMRR, and (d) phase error of the 90° optical hybrid (dark curve is the averaged value over 22 dies, and light-colored region indicates the 1-δ deviation).

CMRR. For the one measurement, phase error extracted from an MZ-delay interferometer spectrum does not depend on absolute GC loss nor GC center wavelength. In the loss and CMRR measurement, the on-chip light after the GC is first split by a Y-junction with a 50:50 splitting ratio. One branch of the Y-junction goes into the LO/signal port of the hybrid. The four output ports of the hybrid are connected to four on-chip photodetectors. The other branch of the Y-junction goes into a fifth on-chip photodetector for calibration. We extracted the loss and CMRR of the hybrid by subtracting the photocurrent of each of the four photodetectors from that of the calibration photodetector. In both cases, variation in the GC does not propagate into the measurement.

To verify the uniformity of the 90° optical hybrid after fabrication, we run automated tests on 22 dies across one 8-inch wafer. To the best of our knowledge, this is the first time that the statistics of the fabricated 90° optical hybrid have been reported. Fig. 3.5(a) shows the measured total insertion loss of the 90° optical hybrids. The

solid lines are the average total insertion loss over 22 dies, and the light-colored bars represent the 1-δ deviation (68% of the data values are within 1-δ deviation from the average value). The average loss is less than 0.5 dB for both signal and LO inputs across the entire C-band. Even considering a 1-δ deviation, the worst-case insertion loss is less than 0.6 dB. Fig. 3.5(b) illustrates the measured imbalance of both the in-phase (I) channel and the quadrature (Q) channel. The average imbalance is better than 0.25 dB across the C-band. When considering the 1-δ deviation, the worst-case power imbalance is less than 0.35 dB. Fig. 3.5(c) shows the measured CMRR of both the in-phase channel and the quadrature channel. The average CMRR is larger than 31 dB across the C-band. Even considering a 1-δ deviation, the worst-case CMRR is larger than 28 dB. Fig. 3.5(d) shows the measured phase error. The averaged phase error is between 0° and -1°. The 1-δ phase error deviation falls between -3° and 3°, indicating the excellent phase control of this 90° optical hybrid.

Fig. 3.6 shows the measured performance of the 90° optical hybrid on a single die. We see that this 90° optical hybrid achieves an insertion loss of less than 0.45 dB, with phase errors smaller than 2° and CMRR larger than 30 dB over the C-band.

3.3.2.2 Packaged Coherent Receivers

Fig. 3.7(a) shows the schematic diagram of a packaged coherent receiver. To measure the phase error of the packaged coherent receiver, light at two different frequencies is input to the signal and LO ports respectively. These two frequencies pass through the 90° optical hybrid and beat in the PDs, generating sinusoid waves at the I and Q ports. The sinusoids are then amplified by the trans-impedance amplifiers (TIAs) and captured on a high-speed oscilloscope. Fig. 3.7(b) shows the measured voltages of the I and Q ports.

Phase difference between I and Q ports is then calculated in the time domain at different frequency offsets as shown in Fig. 3.7(c). The dots indicate the measured phase difference at different frequency offsets, and the solid line is the linear fitting of the dots. Phase error is calculated by subtracting 90° from the y-intercept. Fig. 3.7(d) shows the measured phase error over the C-band. The measured phase error of the packaged coherent receiver is smaller than 3° which matches well with the measurement of the standalone device as shown in Fig. 3.5(d).

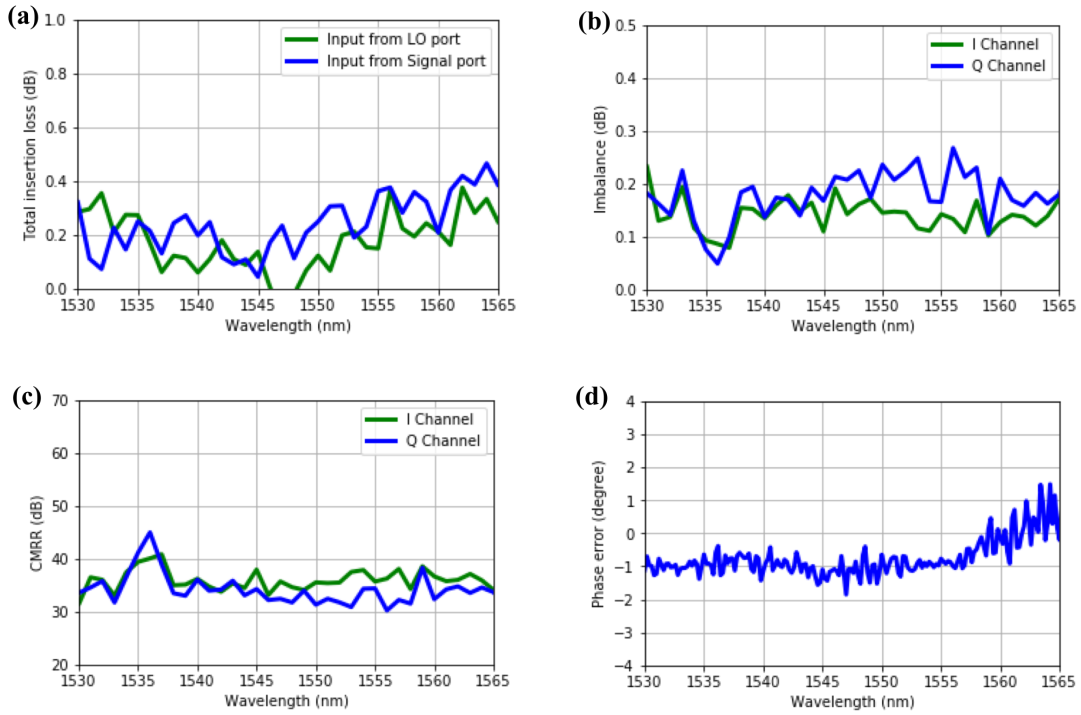


Figure 3.6: Measured (a) total insertion loss, (b) imbalance, (c) CMRR, and (d) phase error of the 90° optical hybrid on a typical die.

3.4 Discussion

The proposed 90° optical hybrid has five advantages over previous devices: (1) it does not use 2×4 MMI couplers or 4×4 MMI couplers, resulting in a drastically reduced footprint, (2) it has lower loss, because its geometry is fully optimized using PSO, (3) it reduces the mode number and the length of the multimode region, thus reducing the phase error, (4) it does not require a waveguide crossing at the output as conventional Type-I devices do, thus reducing crosstalk, and (5) it is resilient to process deviation and therefore suitable for high-volume manufacturing.

To investigate the influence of the CMRR and loss of a 90° optical hybrid to the overall coherent receiver performance, we simulate a receiver to find the required optical signal-to-noise ratio (OSNR) needed to achieve a bit error rate (BER) of 2×10^{-2} in a typical coherent receiver under different CMRR and insertion loss values for the 90° optical hybrid. Contour curves of the results are shown in Fig. 3.8. The simulation is executed in a MATLAB environment with a model of the hybrid that includes excess

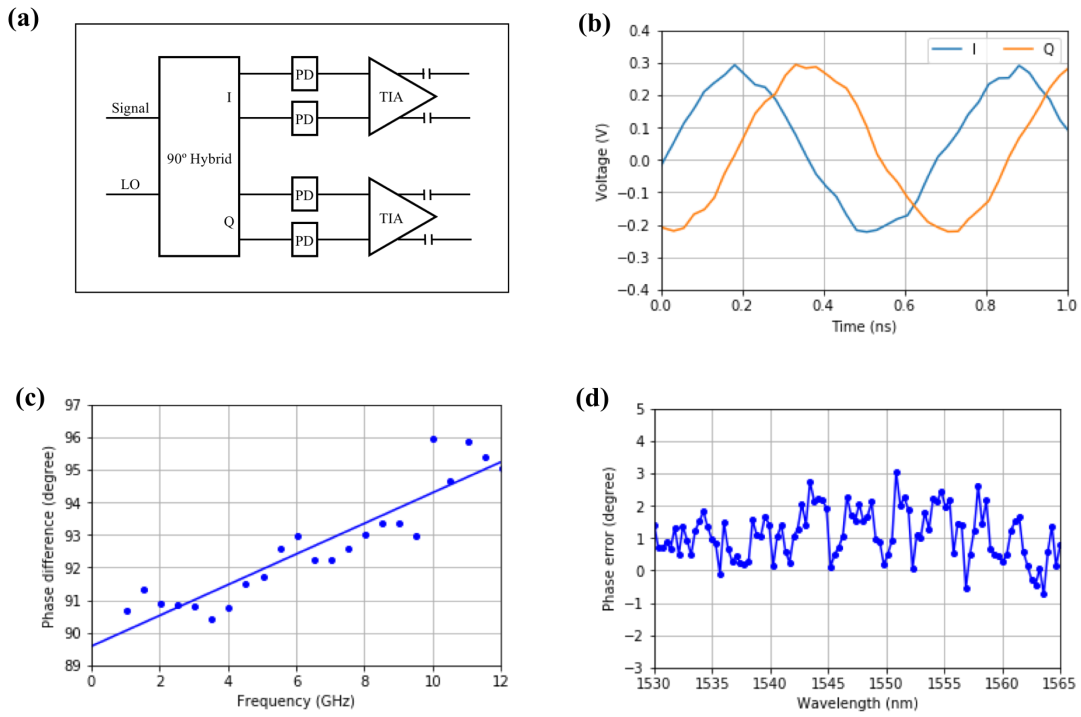


Figure 3.7: (a) Schematic of the coherent receiver module. (b) Measured output voltages after TIAs as a function of time. (c) Measured phase difference between the I and Q channels as a function of beating frequency at 1550 nm. (d) Measure phase error in the entire C-band.

loss, phase error, and CMRR. Models of the transmitter and receiver are consistent with current generation transponder designs. The input is a 16-QAM dual-polarization signal at a speed of 34 Gbaud and a power of -18 dBm. The input also includes 8 adjacent "aggressor" channels each with a power of -4.5 dBm on 50 GHz grid and a 200 GHz gap on each side of the selected channel. Note a phase error within 5° can be corrected by the digital signal processor (DSP) without OSNR penalty in our simulation. Fig. 3.8 shows that for low hybrid losses, CMRR dominates the required OSNR. For example, at a hybrid loss of 0.5 dB, the required OSNR improves ∼4 dB when the CMRR of the hybrid improves from 20 dB to 30 dB. This result is significant because a 3-dB improvement in OSNR essentially doubles the reach of the optical channel. For a CMRR higher than 25 dB, hybrid loss has more impact on OSNR but the margin of improvement is not significant.

Table. 3.2 compares the results of our work with other published 90° optical hybrid

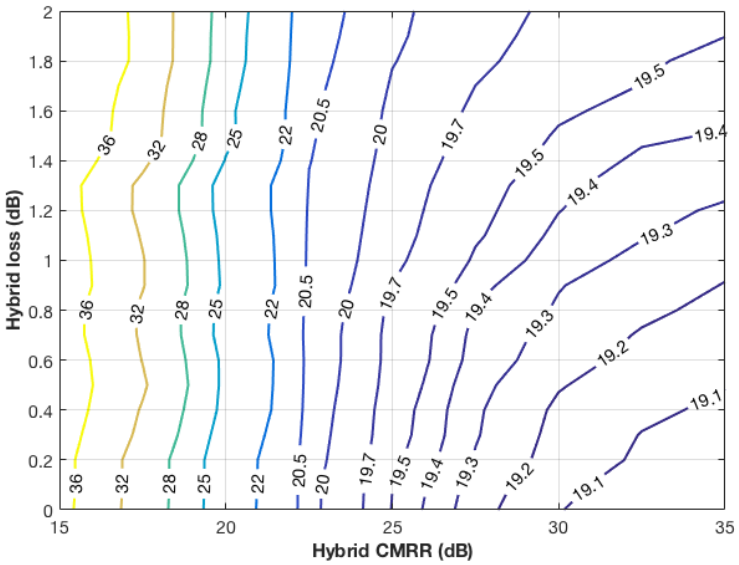


Figure 3.8: Simulation results shown as contours of the required OSNR for a 16 QAM coherent receiver for different CMRR and insertion loss values of 90° optical hybrid.

results. Only our work shows measurement results for more than 20 devices across one wafer. All other works show only the measurement result of a single device. Loss, phase error, and CMRR are all worst-case results in the C-band. Our device achieves the most compact footprint, with other metrics (loss, phase error, CMRR) better than or comparable to the state-of-the-art results.

Reference	**[265]**	**[272]**	**[271]**	**[263]**	**[266]**	**This Work**
Publication Date	2010	2011	2011	2011	2013	2017
Material	InP	SOI	InP	SOI	SOI	SOI
Type	2x4 MMI +2x2 MMI	Shallowly-etched 4x4 MMI with two inputs	Tapered 2x4 MMI +2x2 MMI	4x4 MMI	Wedge-shaped 2x4 MMI +2x2MMI	PSO-optimized 2x2 MMI
Size (μm × μm)	18x379 (6,822)	12x115.5 (1,386)	18.6x227.9 (4,078)	10x185 (1,850)	12x107 (1,284)	21.6x27.9 (602)
Loss (dB)	1.5	N.A.	N.A.	0.5	1	0.45
Phase Error (∘)	5	5	7	5	5	2
CMRR (dB)	30	15	20	20	20	30

Table 3.2: Performance comparison of 90° optical hybrid.

3.5 Conclusion

We experimentally demonstrated a 90° optical hybrid with a footprint of 21.6 μm × 27.9 μm on a SOI platform. Our hybrid consists of a Y-junction and three 2×2 MMI couplers optimized using PSO. The fabricated hybrid exhibits an insertion loss less than 0.5 dB, with phase errors smaller than 3° and CMRRs larger than 30 dB over the C-band.

Part II

Lasers and Transceivers

Chapter 4

Polarization-Insensitive WDM Receiver for Data Center Connectivity

This chapter is about a polarization-insensitive 40Gb/s 4-WDM channels receiver on SOI platform. The notable contributions of this work are:

- The receiver achieves a 160 Gb/s aggregate data rate.
- The polarization-dependent loss of the receiver is less than 1.2 dB with no measurable polarization-dependent wavelength shift.

4.1 Silicon Photonic Transceivers in Data Centers and HPC

Silicon-on-insulator (SOI) integrated photonics is a very promising platform for next-generation optical interconnects and telecommunication systems [281]. Silicon waveguides provide large refractive index contrast enabling small device footprints. In addition, the platform is compatible with the complementary metal-oxide-semiconductor (CMOS) infrastructure to allow for very high-volume manufacturing at high yield because of the stable, consistent materials and methods in a CMOS fab. [282]. However, waveguides with strong optical confinement usually exhibit large birefringence, which

poses a challenge to many applications. Particularly for receivers, large polarization-dependent wavelength shifts (PDWSs) among demultiplexed wavelength channels can lead to undesirable signal distortions. To address this issue, a polarization compensation scheme may be used to align the responses for different polarizations when the channel spacing is large, such as coarse wavelength-division multiplexing (CWDM) [236, 283, 284, 285]. However, fabrication errors in the waveguide widths may cause additional PDWS in this scheme. Alternatively, one can use a polarization transparent or polarization diversity scheme [229, 286] that separates the two orthogonal polarizations, and then utilizes two separate demultiplexers to drop off individual wavelength channels. Here we demonstrate a polarization-insensitive WDM receiver based on a novel bi-level Y-junction that could achieve ultra-low polarization-dependent loss (PDL) [238].

4.2 Receiver Design

Fig. 4.1(a) shows the layout of the receiver chip. It includes a bi-level Y-junction, two 1×4 Mach-Zehnder Interferometer (MZI) based demultiplexers, six monitoring diodes, and four gain-peaked, high-speed germanium photodetectors (PDs) [287].

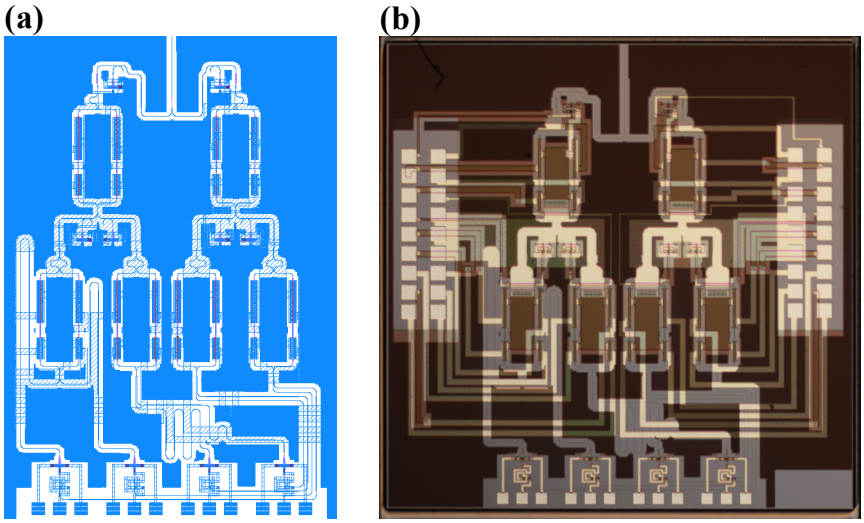


Figure 4.1: (a) Layout of the receiver chip without showing the metal wire and pads that are used to bias the MZIs. (b) Chip image.

The input optical signal with both TE and TM light, is first coupled to the chip via an inverse nano-taper, and then is split by the bi-level Y-junction to two TE modes. Each of the TE modes then enters an MZI based demultiplexer to be separated according to WDM channel number. Finally, the two signals which were originally TE and TM for one wavelength at the input, are combined in a gain-peaked PDs from opposite directions. Since both TE and TM components of the input signal will be converted to TE mode by the bi-level Y-junction for subsequent processing, the PDWS is eliminated. Any PDL would accumulate from the difference in the optical paths prior to the signals arrival at the inputs of demultiplexers, i.e., insertion losses of fiber coupling. Fig. 4.1(b) is a microscope image of a fabricated chip. The chip has a footprint of 2.4 mm $\times$ 2.4 mm, and is fabricated an 8-inch SOI wafer, consisting a 220 nm thick silicon film on top of a 2 μm thick buried oxide layer (BOX) [234].

4.3 Receiver Characterization

4.3.1 PDL Measurement

The experimental setup for performance evaluation is illustrated in Fig. 4.2.

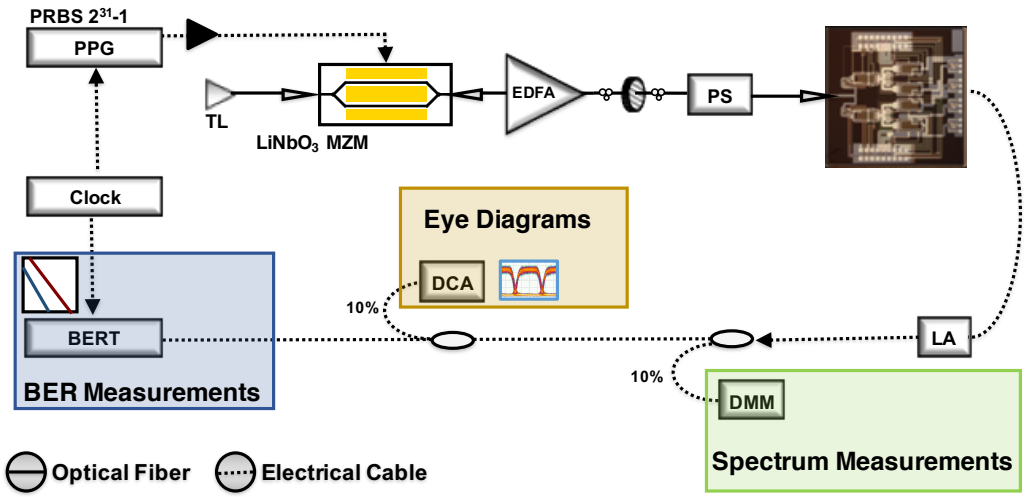


Figure 4.2: Experiment setup for performance evaluation.

In our setup, a continuous-wave (CW) tunable laser (TL) signal was modulated with a pulsed-pattern generator (PPG) to produce a non-return-to-zero (NRZ) 2^{31}-1 pseudo-random bit sequence (PRBS) signal. That signal was then amplified by an

erbium-doped fiber amplifier (EDFA). The amplified light was further passed through a polarization controller (PC) and a polarization scrambler (PS) before edged-coupled onto the receiver chip (the device under test or DUT) using a tapered fiber. A digital multimeter (DMM) was used to record the photocurrent from the gain-peaked PDs and a limiting amplifier (LA) was used to amplify the photocurrent. One output from the LA went to a BER tester (BERT), and the other output went to a digital communications analyzer (DCA) to record eye diagrams.

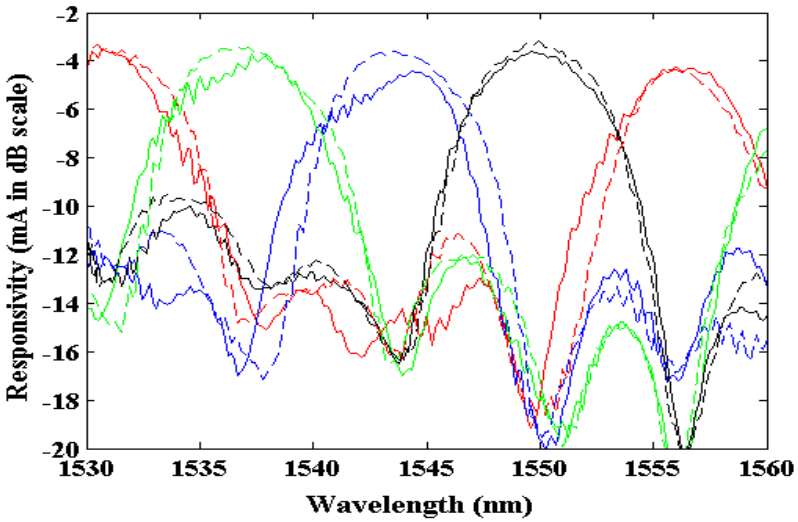


Figure 4.3: Spectra of four channels at the lowest-loss polarization state (dashed line) and the highest-loss polarization state (solid line).

We first tuned the demultiplexers in the two branches, so their pass-bands are correctly aligned. After the alignment, the spectrum of each channel should be relatively stable regardless of the state of polarization (SOP) of the input light. Fig. 4.3 shows the measured spectra at the lowest-loss (maximum responsivity) and highest-loss (minimum responsivity) SOPs. The worst-case PDL is about 1.2 dB and the worst-case crosstalk level is about 9 dB.

4.3.2 40 Gb/s NRZ-OOK Data Transmission

We next characterized the electrical eye diagram of the receiver chip at each channel with data rate of 40 Gb/s. Fig. 4.4(a) shows the received electrical eye diagrams of all four channel when the input state of polarization is fixed. Clean and open eyes

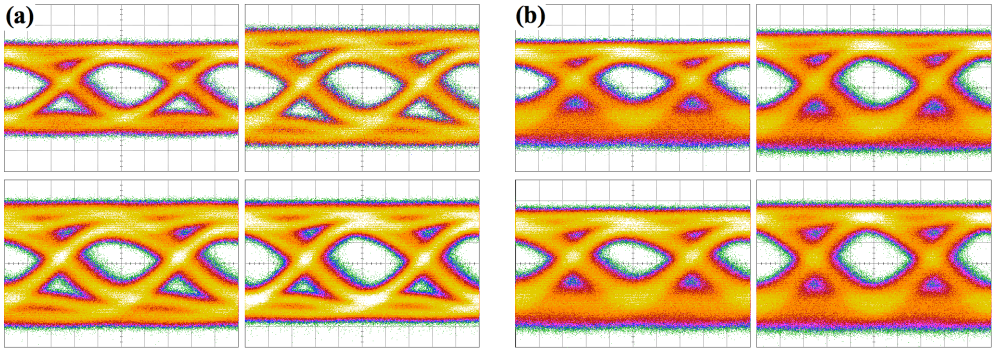


Figure 4.4: Received electrical eye from all channels at 40 Gbps (a) without (b) with scrambled polarization (3 mV/div, 5 ps/div).

are observed for all four channels. Fig. 4.4(b) shows the measured eye diagrams when scrambling of the input polarization is scrambled.

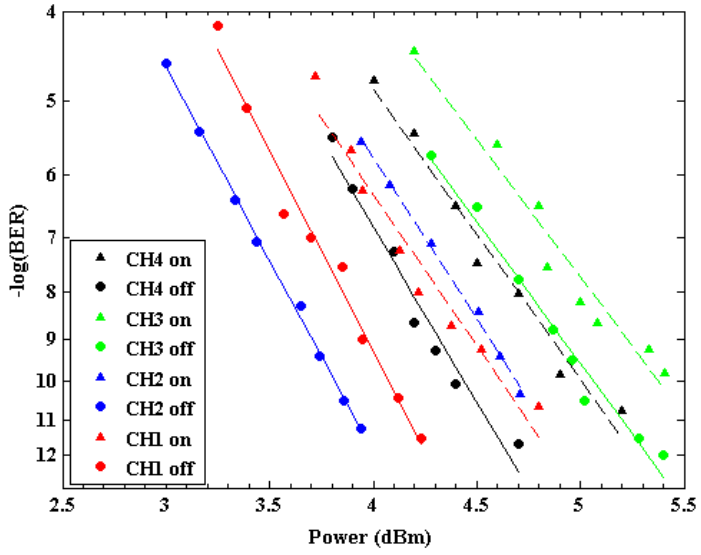


Figure 4.5: Experimental results of BER measurements at 10 Gbps. Dashed and solid lines represent when the scrambler is on and off, respectively.

Lastly, we characterized the bit-error ratio (BER) as a function of coupling power to the chip at each channel with data rate of 10 Gb/s due to the limitations with available test equipment. Fig. 4.5 shows the measured BER vs. power results of all four channels when turning on or off the scrambler. Error-free data transmission (BER $< \times 10^{-12}$) was achieved for all four channels when the polarization scrambler was off.

A maximum BER power penalty of 0.9 dB was observed when activating the scrambler, measured at a BER of $\times 10^{-9}$.

4.4 Discussion

Table. 4.1 compares the performance of our work with other published PI-WDM receivers. The demonstrated receiver achieved the highest single channel data rate and aggregate data rate so far.

Reference	**[288]**	**[284]**	**[286]**	**[289]**	**[290]**	**This Work**
Publication Date	2011	2012	2014	2016	2017	2015
Number of Channels	8	10	5	4	4	4
Channel Spacing (nm)	20	0.8	5	5	1.6	6.5
Single Channel Data Rate (Gb/s)	2.5	10	20	25	25	40
Aggregate Data Rate (Gb/s)	20	80	100	100	100	160
WDM Method	Si_3N_4 PI-AWG	Si_3N_4 AWG	2nd-order-ring based Demux	Ring based Demux	2nd-order-ring based Demux	MZI based Demux
Polarization Handling Method	Si_3N_4 PI-AWG	PSR	PSGC	PSGC	PBS	PSR
PDL (dB)	1.2	1.8	0.5	0.5	0.5	0.7
PDWS (nm)	1.9	0	0	0	0	5

Table 4.1: Performance comparison of recent silicon photonic PI-WDM receivers.

4.5 Conclusion

We demonstrate a polarization-insensitive WDM receiver chip with 4 wavelength channels at 6.5 nm spacing. The receiver chip includes a bi-level Y-junction, four gain-peaked germanium PDs, and two MZI-based de-multiplexers. The receiver chip is shown to have less than 1.2 dB PDL, and no PDWS. Operation at 40 Gb/s with scrambled polarization is demonstrated for all four channels.

Chapter 5

III-V/Silicon Hybrid External-Cavity Laser for Coherent Communication

The work in this chapter describes a III-V/silicon hybrid external cavity laser with a tuning range larger than 60 nm in the C-band on a silicon-on-insulator platform. A III-V semiconductor gain chip is hybridized into the silicon chip by edge-coupling the silicon chip through a S_3N_4 spot size converter. The demonstrated packaging method requires only passive alignment and is thus suitable for high-volume production.

The notable contributions of this work:

- The laser has an output power of 11 mW (in the exit waveguide) with a wall-plug efficiency of 4.2%, tunability of 60 nm (more than covering the C-band), and a side-mode suppression ratio of 55 dB (>46 dB across the C-band).

- The lowest measured linewidth is 37 kHz (<80 kHz across the C-band), which makes this laser acceptable for coherent communication.

- Experimental demonstration of all-silicon-photonics-based transmission of 34-Gbaud (272 Gb/s) dual-polarization 16-QAM using our integrated laser and a silicon photonic coherent transceiver was successfully conducted. The results show no additional penalty compared to commercially available narrow linewidth tunable lasers.

- First experimental demonstration of a complete silicon-photonic-based coherent link.

5.1 Silicon Photonic Transceivers in Telecommunications

Silicon photonic (SiPh) devices have gained significant market traction in metro, data center interconnect, and intra-data center applications, and are widely viewed as a key technology for next-generation networks which will require high data rates, high density, energy efficiency, and low cost [5, 70, 291, 292]. This technology can be used in a wide range of applications from short-reach interconnects [61, 69, 293] to long-haul communications [60, 62, 75, 77, 78]. However, practical silicon-based light sources are still missing, despite the progress in germanium lasers [294, 295]. Both silicon and germanium are indirect-band semiconductors and inefficient at light generation. This situation has propelled the study of III/V-based laser integration in a silicon-on-insulator (SOI) platform.

Laser integration approaches fall into three general categories: monolithic, heterogeneous, and hybrid. Monolithic integration involves the direct hetero-epitaxy of III-V materials [296, 297, 298]. Heterogeneous integration consists of the attachment of unprocessed III-V material to a silicon chip or wafer and the subsequent co-fabrication to form a laser [45, 208, 299, 300, 301]. Hybrid integration refers to the integration of a finished gain chip with a silicon chip or silicon wafer [302, 303, 304, 305, 306, 307, 308, 309, 310, 311].

5.2 Laser Design

5.2.1 Laser Architecture

The tunable laser is constructed with a passively bonded reflective semiconductor optical amplifier (RSOA), a spot-size converter (SSC), and a reflective external cavity built from ring resonators [312, 313]. The schematic of the III-V/silicon hybrid laser is shown in Fig. 5.1. For this work, we use a 600 m long Indium-Phosphide (InP) multi-quantum-well (MQW)-based RSOA as a gain material. The output waveguide of the RSOA is angled by 9° and anti-reflection coated to reduce the back reflection at the facet. The rear facet of the RSOA is coated with a high reflectivity (HR) coating.

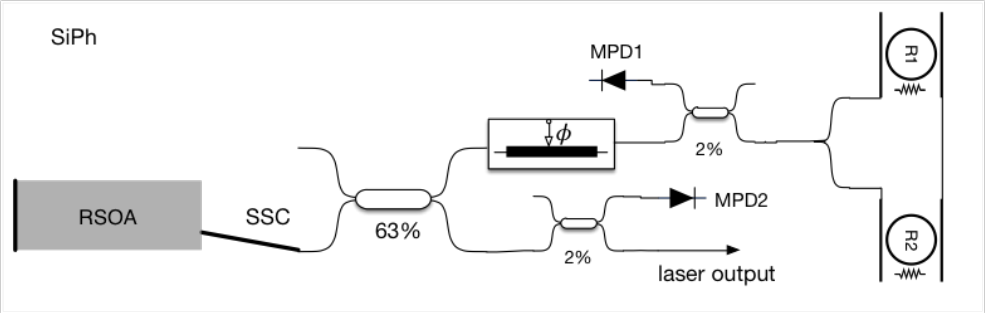


Figure 5.1: A schematic view of the tunable laser.

The SSC is implemented to provide mode-matching between the RSOA and the silicon waveguide. The SSC is also angled to match the RSOA output angle and further reduce reflection at the facet. A directional coupler (DC) is connected to the SSC in order to split 37% of the power to the laser output port and 63% (or -2 dB) to the external cavity. For this prototype, a high coupling ratio is chosen to guarantee enough feedback provided by the external cavity and achieve lower threshold currents. On a production level, the coupling ratio can be optimized to trade for higher laser power.

A dual-ring Vernier filter is put at the end of the external cavity to form a tunable reflective filter with a wide tuning range. The dual-ring structure is connected to a Y-junction to form an inline reflector. The Y-junction with dual-ring as a whole can be regarded as a wavelength-selective reflector (WSR). Compared to dual-ring designs with Sagnac loop mirror at the end [308], light travels in the WSR only once, reducing the round-trip loss by a half and hence increasing the feedback amplitude. A phase tuner is included before the WSR to fine-tune the longitudinal modes of the laser cavity to align one with the peak of the WSR, in order to control mode hop behavior. Between the WSR and phase tuner, a 2% DC tap to a monitoring photodetector (MPD) allows us to monitor the feedback within the external cavity. The total routing waveguide length on the silicon photonics chip is $\sim$1100 μm, which results in the simulated longitudinal laser mode spacing of $\sim$0.18 nm.

5.2.2 Spot-Size Converter

Due to the large mode mismatch between the RSOA waveguide and silicon waveguides, we introduce an optical spot-size converter on the silicon photonic chip to reduce the coupling loss between the chips. The SSC uses a layer of silicon nitride (Si_3N_4) which

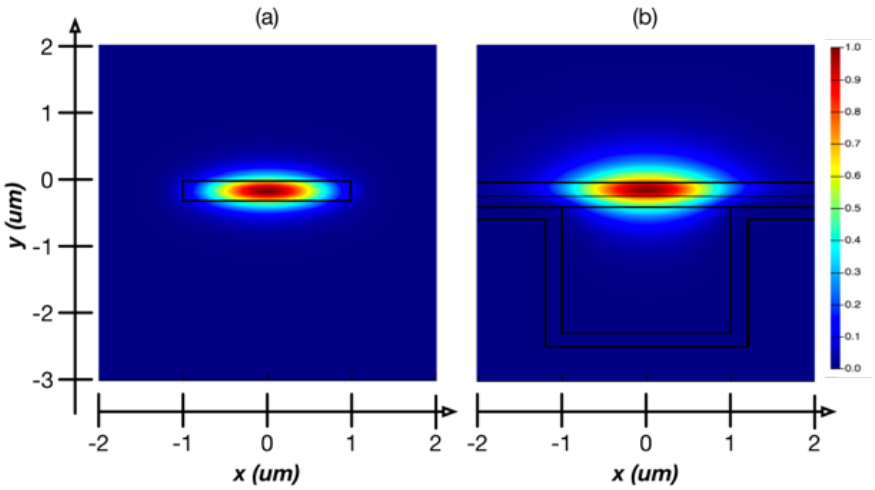


Figure 5.2: Magnitude of the electric field for the silicon nitride waveguide (a) on the silicon photonic chip, and (b) for the RSOA chip.

reduces the waveguide-to-cladding index contrast to $\Delta n \approx 0.5$ (Si_3N_4/SiO_2), in comparison to a standard silicon waveguide, $\Delta n \approx 2$ (Si/SiO_2). The smaller index contrast of the Si_3N_4 waveguide results in a larger mode, which enables greater mode matching to the RSOA mode. Simulation results in Fig. 5.2 show how the electric field of the Si_3N_{43} waveguide (a) is comparable to the mode of the SOA chip (b), here the mode-mismatch loss is only -0.18 dB representing a 96% mode overlap. The SSC coupler design adiabatically transforms the high confinement silicon ridge waveguide into the Si_3N_4 waveguide shown in Fig. 5.2(a). This coupler uses multiple Si_3N_4 layers from the back end of line and has an experimentally measured efficiency of (0.73±0.06) dB.

Although the mode mismatch between the modes can be small, practically the coupling loss is higher given misalignments and the presence of a small gap between the two chips. In Fig. 5.3, we can see that an additional 1 dB of loss can arise from a misalignment of either 0.50 μm in the horizontal, or 0.25 μm misalignment in vertical direction. Further, the space between the chips contributes 1 dB per micron of gap assuming the interface is using index matching gel or epoxy. The misalignment in the vertical direction (y) is typically small and on the order of 0.1 μm since it depends on the position and thickness of the hard stop layer which can be accurately monitored by the fabrication process. The accuracy in the horizontal as well as the gap between the chips is determined by the accuracy of the chip placer which is on the order of 0.5 μm

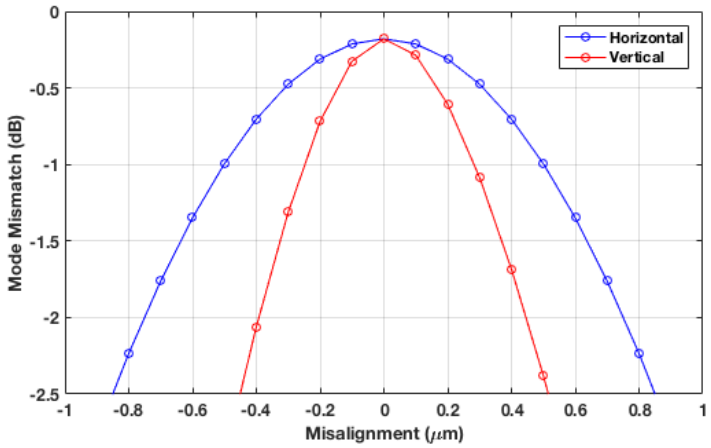


Figure 5.3: Mode mismatch between the silicon photonics chip and the SOA as a function of misalignment in the horizontal (x) and vertical direction (y).

for 3-sigma placement accuracy.

5.2.3 External Double-Ring Resonator Laser Cavity

The ring resonator layout is similar to the work [314]. The add-drop ring resonator performance is simulated by analytical formula [138, 315] with parameters extracted from experimental data. One ring resonator has a bend radius of 20 μm (R1) and an FSR of 4.99 nm near 1550nm. The measured Q-factor is 5500. The other ring resonator has a bend radius of 16.3 μm (R2) and an FSR of 6.13 nm near 1550nm. The measured Q-factor is 4800. The Vernier ring reflected spectrum is plotted in Fig. 5.4(a). When the rings reflection is tuned to 1570 nm, the side mode extinction is larger than 8 dB across a 60nm range (1510 nm - 1570 nm), more than sufficient to operate over the entire C-band. Q-factor of the highest peak (where threshold condition is met) is about 8000.

The simulated and measured reflected spectra of each of R1 and R2 are shown in Fig. 5.4(b). We observe excellent agreement between simulation and experiment. The experimental data (with grating coupler envelope de-embedded) is measured on wafer-scale through grating couplers, and is hence limited from 1525nm to 1575nm, due to the degradation of grating coupler efficiency on edge wavelengths. Out of this range, the measured extinction ratio of ring resonances becomes limited by the power-meter noise floor, which affects the modeling accuracy in simulation. With the extracted

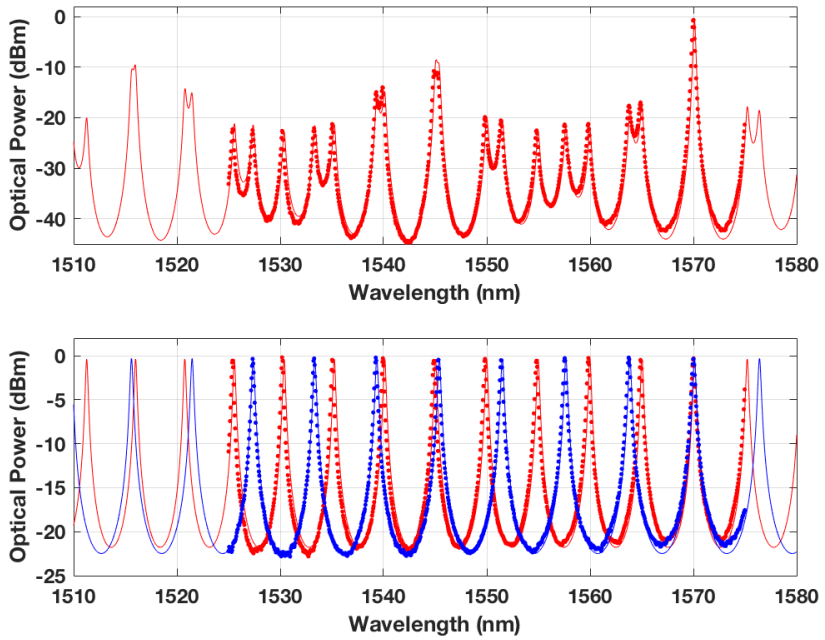


Figure 5.4: (a) Reflected spectra of the Vernier ring, normalized to the maximum power of the reflected spectra. The red line is the simulated spectrum, while the red dots are the measured spectrum. (b) Reflected spectra of R1 (red) and R2 (blue), separately. The solid lines are the simulated spectra, and the red dots are measured spectra.

ring models, we also aligned the reflection peak to other wavelengths from 1510 nm to 1570 nm and observed >8 dB side mode extinction ratio in all cases. The spectra at different wavelengths are slightly different from a shifted spectrum of Fig. 5.4(a), due to dispersion in the silicon waveguides. With >8 dB side mode extinction ratio and 60nm tuning range, the dual-ring design is readily integrated with a RSOA to build a stable, C-band tunable, single mode laser.

5.3 Laser Fabrication and Integration

The silicon photonic chip was fabricated at a complementary metal-oxide-semiconductor (CMOS) foundry using standard CMOS processes. The substrate is an SOI wafer with a 220-nm silicon layer over 2.5 μm BOX . Front end etching and doping processes are used to build the waveguides and active components. Silicon nitride is deposited and patterned in the backend to form the spot size converter to the InP chip as shown in Fig. 5.5(a) as well as a hard stop layer for vertical alignment, shown in Fig. 5.5(b).

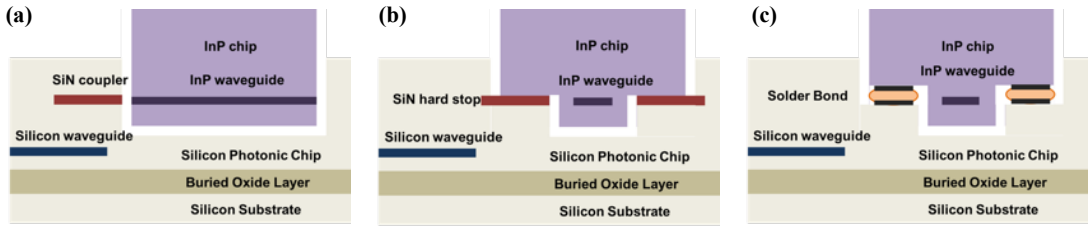


Figure 5.5: Cross sections showing the InP chip integration with the silicon photonics chip (a) along the optical axis, (b) across the optical axis showing the hard stop and (c) across the optical axis showing the electrical bond.

Etched cavities were formed on the silicon photonic chip with mechanical features that matched the InP chip. Eutectic gold-tin (AuSn) solder was electroplated onto the metal contacts to enable chip-to-chip bonding.

The InP RSOA chip was built in a III-V foundry using standard III-V processing techniques. A series of etches define the hard stop at the MQW layer as well as a recessed gold contact pad for bonding with the locations of matching features on the silicon photonic chip. The InP wafer was cleaved into bars which were HR coated on the backside and anti-reflectivity (AR) coated on the front side, to an index of 1.45. The bars were then cleaved into chips comprising two channels each.

InP integration onto the silicon photonic chip was accomplished using a high-precision thermo-compression bonder with placement accuracy of ± 0.5 μm. Vertical

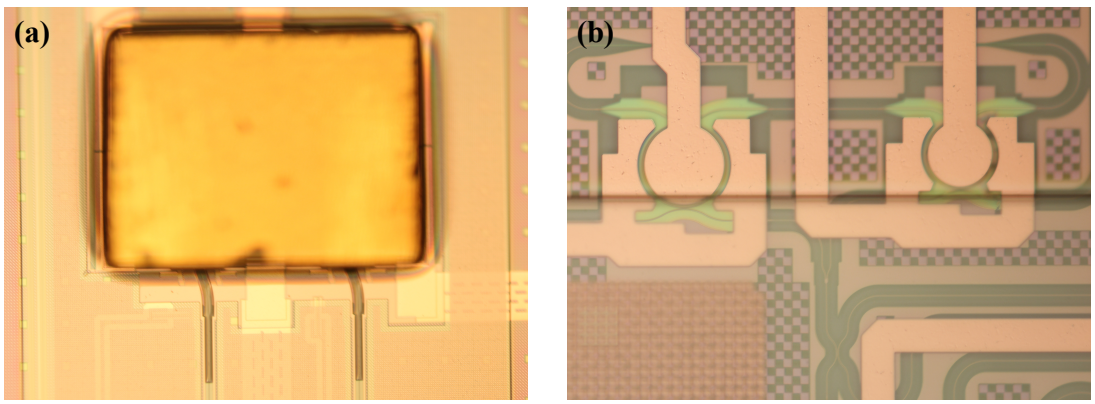


Figure 5.6: (a) Optical image showing the III-V die (face down due to flip-chip bonding) and waveguide couples. Two laser channels are aligned and packaged simultaneously. (b) Optical image showing the Vernier ring reflector. The left ring resonator has a radius of 20 μm (R1), and the right ring resonator has a radius of 16.3 μm (R2).

alignment was accomplished using the hard stop features on both the silicon photonics and InP chips while angular and in-plane alignments were accomplished using the bonder's vision system which utilized alignment features defined on both chips. Fig. 5.6 shows the optical images of the fabricated chips.

5.4 Laser Characterization

5.4.1 L-I-V

The investigated device can be tuned across the C-band to any wavelength, including the ITU channels. Fig. 5.7(a) shows the L-I-V (Light-Current-Voltage) curves of the laser with the lasing wavelength at 1546.88 nm (193.8 THz). The lasing threshold is seen to be 30 mA. Wall-plug efficiency (WPE) can be determined by dividing the on-chip power by the amount of power going into driving the RSOA chip. As shown in Fig. 5.7(b) the ECL achieves peak WPE of 4.2% around an injection current of 90 mA.

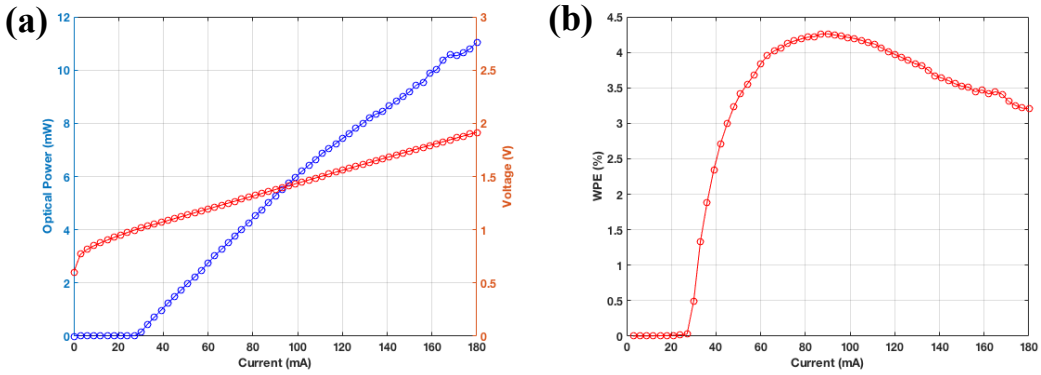


Figure 5.7: (a) L-I-V curve of hybrid laser. Blue and red curve are L-I and I-V curves correspondingly. (b) Extracted experimental WPE. (at 1546.88 nm).

A major challenge for III-V/silicon hybrid external cavity lasers is overcoming wavelength drift and mode-hopping during the laser life [316, 317]. An example showing both wavelength drift and mode-hopping can be seen in Fig. 5.8(a), where the laser spectrum is plotted as a function of injection current, without employing any ring or phase tuning. The lasing wavelength is seen to drift until it mode hops around 160 mA by 0.1 nm to the next longitudinal mode. The wavelength change at the mode hop is smaller than the laser longitudinal mode spacing calculated in the previous section,

similar to earlier observations [303]. Additionally, the wavelength drift before the mode-hop (or between the two mode hops) is larger than laser longitudinal mode spacing. The reason is that as RSOA current increase, not only does the RSOA temperature increase, but also the Si temperature slightly increases resulting in red-shifted ring wavelengths. Both wavelength drift and mode-hopping can be prevented by aligning the rings and phase sections for a given injection current.

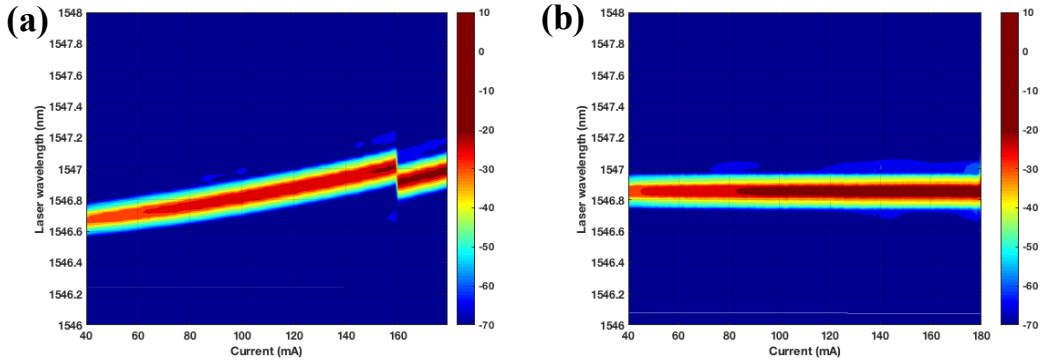


Figure 5.8: (a) Spectral-L-I data without wavelength stabilization. (b) Spectra-L-I data with wavelength stabilization control.

To obtain the graph shown in Fig. 5.8(b) we tune the two rings (R1 and R2) and the phase shift element (PS0) for every value of the injection current, using thermal phase tuners on each element [318]. The ring powers are initially set to power values corresponding to the desired wavelength (from Fig. 5.9). Properly aligned rings results in maximum reflectivity and hence maximum power on the intra-cavity MPD1. The roughly-aligned rings are then aligned with each other by maximizing the photocurrent reading on the MPD1. The laser cavity phase tuner is then scanned and set to a value that biases the laser longitudinal mode to the center of the double-ring resonance [318]. This way we keep the lasing mode away from mode-hop regions. However, the tuning phase tuner can cause the lasing wavelength to shift, requiring further adjustment of the ring biases. This procedure is repeated iteratively until the measured wavelength exactly matches the target wavelength. For this procedure, we use an optical spectrum analyzer (OSA) to monitor the lasing wavelength as the injection current is increased. This method allows us to tune and maintain the lasing peak around the desired wavelength to within the resolution of the OSA (0.02 nm) for every value of the

injection current, corresponding to a tuning accuracy of ± 1.25 GHz in frequency. Such accuracy is within the tolerance needed in most communications applications (± 2.5 GHz). This procedure is employed to demonstrate a mode-hop and wavelength-drift free LIV as shown in Fig. 5.8(b) and ensure operation at any desired wavelength yet away from mode-hop conditions. Further work is needed to ensure that the wavelength is continuously stabilized during the laser operation.

5.4.2 Tunability

Fig. 5.9 shows the lasing wavelengths under different thermal tuning powers applied to each ring resonators with fixed RSOA drive current of 180 mA. Single-wavelength lasing with a SMSR in excess of 46 dB was obtained across a 60-nm tuning range. The tuning range covers the entire telecommunications C-band. The color plot shows the laser tunability from 1515 nm to 1575 nm. The hue gradient along the diagonal color lines shows that the wavelength can be continuously tuned for much of that region. Each one of the diamonds overlaid on the color plot represents the wavelength of an ITU channel for a 100 GHz ITU grid across the entire C-band. Figure 5.10 also shows that the tuning range of the laser covers the entire C-band.

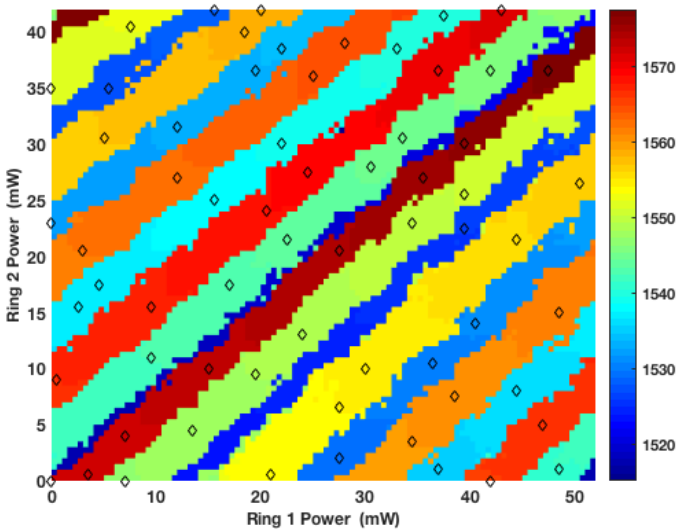


Figure 5.9: Lasing wavelength under different R1 and R2 basing powers. The diamond markers indicate the basing powers at different ITU grid.

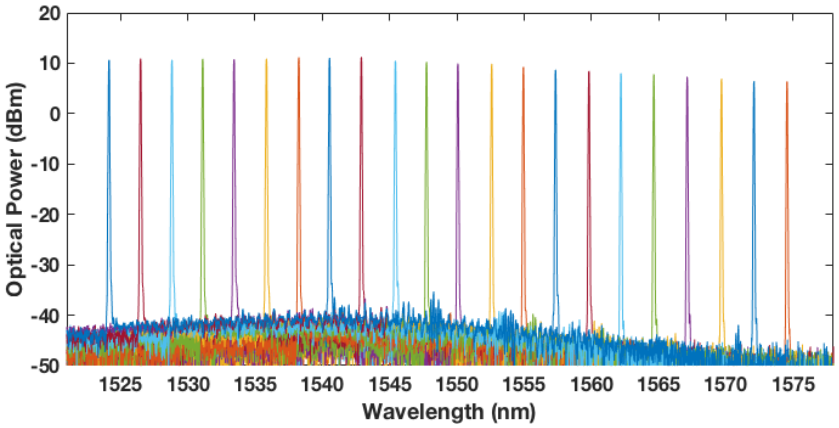


Figure 5.10: Measured lasing spectra of the tunable laser across the C-band.

5.4.3 Spectral Performance

The SMSR was measured at room temperature, with a drive current of 180 mA using an OSA with a resolution of 0.02 nm. The highest measured SMSR was 55 dB, as indicated can be seen in Fig. 5.11(a). Fig. 5.11(b) shows the measured SMSR at different multiple wavelengths from the 100-GHz spaced DWDM ITU grid. The measured SMSR is larger than 46 dB from 1525 nm to 1575 nm, reduced at the edges of the gain bandwidth.

The linewidth of the laser cannot be determined from the spectrum in Fig. 5.11(a), because the laser linewidth is smaller than the resolution of the optical spectrum analyzer (OSA). To measure the linewidth, we use a heterodyne measurement method, similar to delayed self-heterodyne [301, 319]. The output from our laser was mixed with a tunable laser (Keysight N771A) and passed through a coherent receiver. The electrical signal is then observed on a real-time scope. The combined linewidth is analyzed from the FM noise spectrum, by taking the average of the flat region of the noise spectrum (between 20 MHz and 80 MHz) and multiplying by π [319]. The intrinsic linewidth of the reference Keysight laser was measured to be ~40 kHz. The intrinsic linewidth of our ECL laser can be obtained by subtracting the linewidth of the reference laser from the combined value. The measured linewidth for the ECL is below 80 kHz for 7 wavelengths selected as samples across the C-band as shown in Fig. 5.11(d).

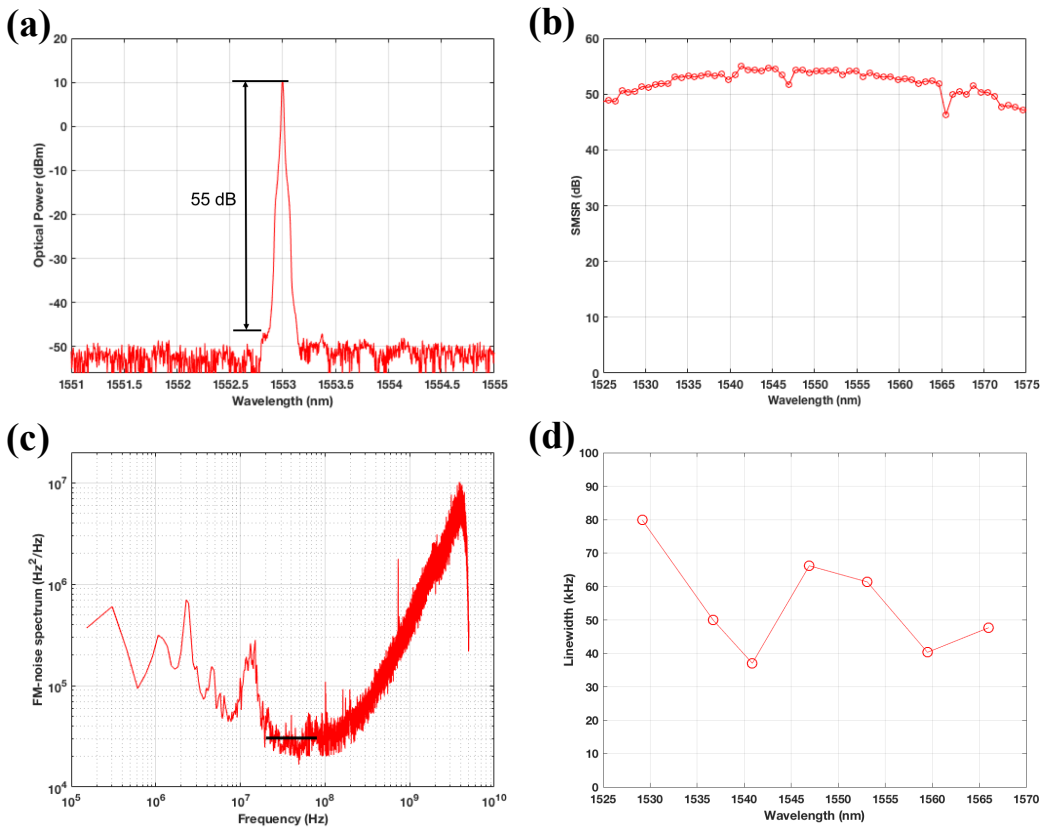


Figure 5.11: (a) Measured laser output power spectrum with the highest SMSR of 55 dB. (b) Measured SMSR at C-band, 100-GHz-spacing DWDM ITU grid. (c) FM-noise spectrum using heterodyne laser linewidth measurement method at 1553 nm. (d) Measured linewidth at different wavelengths across the C-band.

5.5 Coherent Transmission

5.5.1 Experimental Setup

To further evaluate the real-world performance of the laser, a coherent optical transmission experiment is needed [320]. We tested our laser in a noise-loaded, high-speed, dual-polarization (DP), 34-Gbaud, 16-QAM coherent transmission system operating at 272 Gb/s. Fig. 5.12 illustrates the setup used for this test. One highlight of this system is the integrated, silicon photonics-based, integrated modulator/receiver assembly (IMRA). The IMRA houses a silicon photonic integrated circuit (PIC) containing a dual-nested MZ modulator (transmitter) and an optical hybrid. The IMRA also houses

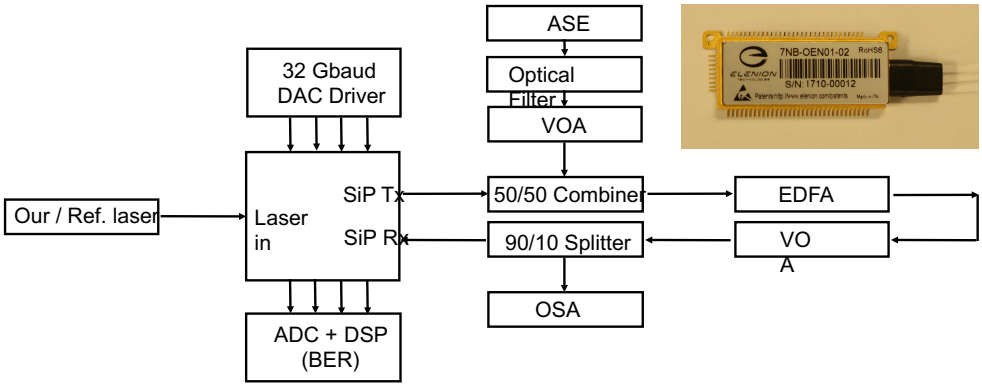


Figure 5.12: 34-Gbaud DP-16QAM experimental setup (main). Image of IMRA (inset).

four low-noise TIAs, which, along with the optical hybrid, form the coherent receiver. The IMRA package has three fibers: one fiber is used for the external CW laser (our laser), which is split on the PIC to serve as both the laser source for the transmitter and the local oscillator for the receiver. The second fiber is used for the output of the optical transmitter (Tx). The third fiber is used for the input signal into the coherent receiver (Rx).

A commercial, four channel, high-speed DAC and driver provided the high-speed 34Gbaud, 16QAM signals driving the DP-MZI modulator. The transmitted 272 Gb/s optical signal was noise-loaded and looped back into the Rx signal port of the IMRA. A commercial high-speed ADC and DSP were used to digitize and process the output signals from the IMRA receiver and measure the bit-error-rate (BER) performance of the system. The noise-loading setup (ASE source, optical filter, and variable optical attenuator (VOA)) allowed us to control the optical signal-to-noise ratio (OSNR). An erbium-doped fiber amplifier (EDFA) and VOA were placed at the Tx output to boost and control the optical power into the receiver. An optical spectrum analyzer measured the signal power and OSNR into the receiver. With this setup, we could measure BER vs. OSNR performance of the transmission system. As shown, our tests were performed in loopback (back-to-back) mode. This configuration was sufficient to test whether the DSP could handle the linewidth of the laser source because the section of the DSP which handles the laser linewidth is separate from the DSP section which handles fiber dispersion. Therefore, for this particular test, it was not critical to propagate the Tx signal over long lengths of fiber.

5.5.2 Experimental Results

In order to assess the performance of our laser source in the coherent system, we made two measurements. First, a reference measurement was made with a commercial tunable laser source (Santur ITLA) suitable for long-haul coherent systems. The CW laser power was 16dBm. The laser wavelength was 1547.2nm. The optical signal power into the receiver was -10dBm. This first measurement provided a baseline BER vs. OSNR curve at -10dBm input into the receiver. For the second measurement, the commercial laser was replaced with our laser source (this work). An EDFA was used to boost the output from our laser to 16dBm.

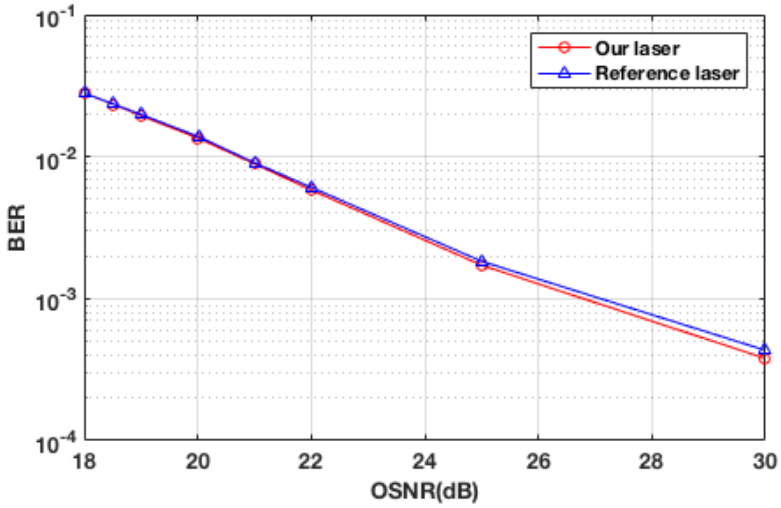


Figure 5.13: Measured BER vs. OSNR at 1547.2 nm.

Fig. 5.13 shows the comparison between the BER vs. OSNR curves measured at 1547.2nm with both the commercial laser and the laser from this work. No noticeable shift was observed between the two curves, confirming the suitability of our laser for coherent transmission applications. Fig. 5.14 depicts the constellation diagrams of the 34 Gbaud dual-polarization 16-QAM using (left) our ECL, and (right) reference laser. The quality of the received signals in both cases are comparable.

5.6 Discussion

The demonstrated III-V/silicon hybrid external cavity laser has three advantages: (1) multiple laser cavities can be passively aligned simultaneously, which is suitable for

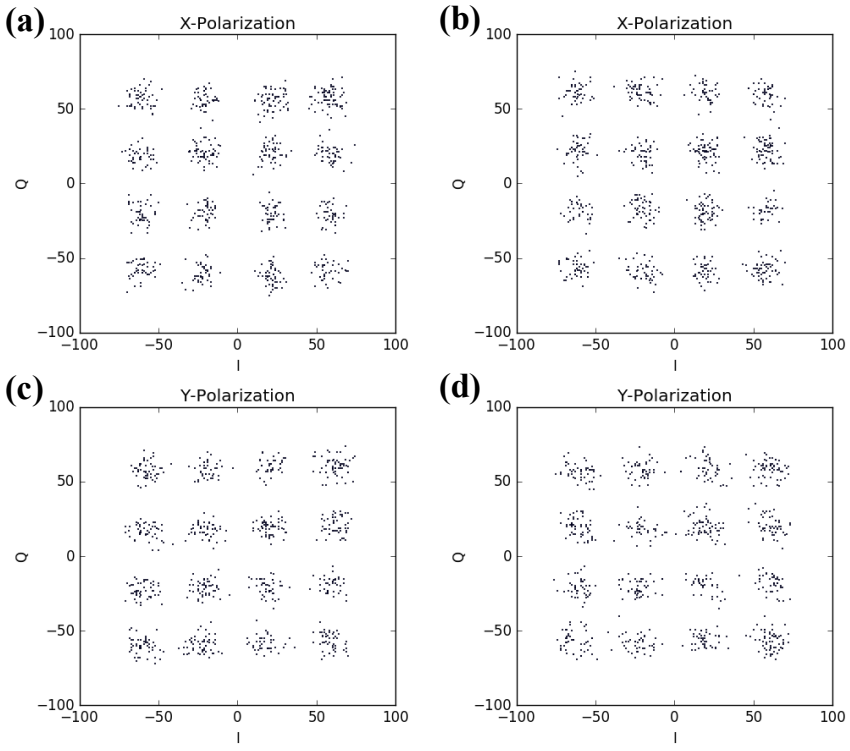


Figure 5.14: Constellation diagram of the 34 Gbaud DP-16 QAM using (a), (c) our ECL, and (b), (d) reference laser.

high-volume production of one or more lasers, (2) the high Q-factor Vernier ring structure provides a wide tuning range and a narrow linewidth, and (3) mode-hop-free operation and wavelength locking operation are achieved by active controls.

Table. 5.1 compares the performance of our work with other III-V/silicon hybrid external cavity lasers. The SMSR and linewidth listed are the best results in the C-band. The stated ower and WPE are the maximum output power and largest wall-plug efficiency. Of these devices, our tunable ECL achieves the largest tuning range by a factor of 2 and the narrowest linewidth by a factor of 5.

5.7 Conclusion

We demonstrate a III-V/silicon hybrid external cavity laser with a tuning range larger than 60 nm in the C-band on a silicon-on-insulator platform. A III-V semicon- ductor gain chip is bonded in an etched well within the silicon chip with its waveguide(s) edge-

Reference	**[304]**	**[301]**	**[299]**	**[321]**	**[322]**	**This Work**
Publication Date	2012	2013	2013	2017	2017	2018
Integration	Hybrid	Hetero-genenous	Hetero-genenous	Hybrid	Hybrid	Hybrid
Alignment	Passive	Passive	Passive	Active	Active	Passive
Coupling	Butt	Butt	Vertical	Free-space	Butt	Butt
Laser Type	Single Ring + DBR	DBR	Single Ring + DBR	Vernier Ring	Si_3N_4 Ring	Vernier Ring
Tunability (nm)	N.A.	>20	8	57	27	>60
Power (mW)	15	8	10	35	1.7	11
WPE (%)	7.6	N.A.	N.A.	N.A.	1.7	4.2
SMSR (dB)	40	40	50	60	60	55
Linewidth (kHz)	N.A.	200	1700	130	17	37

Table 5.1: Performance comparison of recent C-band tunable laser works.

coupled to the silicon photonic waveguide(s). The demonstrated packaging method requires only passive alignment and thus is potentially suitable for mass production. The laser has an output power of 11 mW in the output waveguide with a wall-plug efficiency of 4.2%. and a side-mode suppression ratio as large as 55 dB. The measured linewidth is as narrow as 37 kHz, which is suitable for co- herent communication. In addition, we successfully demonstrate a 34-Gbaud DP-16QAM transmission using our laser and a silicon photonic transceiver on par with the performance of commercially available lasers. To the best of our knowledge, this is the first experimental demonstration of a complete silicon-photonic-based coherent link.

Part III

Reconfigurable Optical Interconnects

Chapter 6

Reconfigurable Silicon Photonic Interconnect for Many-Core Processor Architecture

The work in this chapter includes the design and prototype implementation for Optically Connected Memory Modules (OCMMs) that offer a novel nanophotonics-based approach to adapting bandwidth bottlenecks. The proposed modules can be located up to several meters distant from the CPU, yet supply enough bandwidth to match the performance of the more restrictive Multi-Chip Modules (MCM) approaches. At these high bandwidth densities, the Network-on-Chip (NoC) becomes the primary bottleneck of the architecture, so we organize these memory modules in a reconfigurable nanophotonic interconnect fabric that adapts to memory access patterns. We use architectural simulation of the design to demonstrate the effectiveness of our approach. Finally, we demonstrate a functioning prototype of this new architecture using a tunable laser, a 4-channel silicon photonic de-multiplexer chip and a 4x4 mesh NoC synthesized in a field-programmable gate array (FPGA).

The notable contributions of this work:

- Simulation shows that we can reduce NoC latency by 1.5x and NoC bandwidth overprovisioning between 33-45% for adversarial traffic patterns as long as the re-provisioning time for the photonics is held below 50 ns.

- The demonstrated hardware prototype achieves a 15-ns channel switching time

(well below the 50 ns the simulations required), which demonstrates the feasibility of implementing the proposed processor-memory architecture in the real world.

- This is the first time that reconfigurable silicon photonic interconnects are proposed and partly demonstrated for a processor-memory architecture.
- This work can be considered as a step toward solving the memory access issue in current many-core, many-memory systems.

6.1 Memory Wall

In the last decade, the end of Dennard Scaling has led manufacturers to move towards multi-core chip architectures to circumvent the concomitant clock speed limits that prevent further performance scaling of single core CPUs. Many-core Chip Multiprocessors (CMPs) continue to scale to ever larger "on-chip" capabilities, but these capabilities are increasingly limited by off-chip IO bandwidth, especially accesses to off-chip memories, known as the memory wall problem [323, 324].

Co-packaging of the CMP with stacked memory on silicon carriers or other forms of Multi-Chip Modules (MCM) has enabled scaling of memory bandwidth by increasing pin-densities within the MCM using stacked memory technologies such as High Bandwidth Memory (HBM) and Hybrid Memory Cube (HMC), but at considerable cost and complexity. Furthermore, MCMs have very limited area, which means that although they are able to offer substantial gains in bandwidth, they are unable to offer as much memory capacity as slower off-chip memory approaches such as DDR DIMMs. Breaking out of the MCM using electrical connections is not practical due to the fundamental bandwidth density limitations of electronic interconnects that have been clearly articulated by David A. B. Miller's article [325]. There is an urgent need to break out of the MCM to offer both memory bandwidth and memory capacity and to overcome the cost and packaging density challenges of continuing to scale the size of MCM technologies. We will demonstrate that addressing these challenges is both practical and achievable using a mixed photonic/electronic architecture.

Memory capacities and bandwidth must somehow scale with the compute capabilities of CMPs, and this adds significant pressure to develop better memory interfaces. This pressure, in addition, might be exacerbated by the forecasted end of Moore's Law

[326]. Hence, with transistors available in limited amounts on a single CMP chip, there is an incentive to exploit these transistors as much as possible for compute operations. Forecasts of addressing these memory bandwidth challenges by moving to PIM and non-Von-Neumann architectures ignore the fact that it would further exacerbate the existing memory capacity challenge [327].

This forecasted heavy reliance on off-chip memories requires memory modules to be available in large enough quantities and accessible with sufficiently ample bandwidths and low latencies [328]. These requirements are, however, hard to meet with conventional means. First, the number of IO pins or bumps available to "escape" a chip is limited, both technologically (e.g. difficulty to fabricate pins or bumps of ever smaller sizes) and economically (fabrication and packaging costs balloon as bumps are miniaturized). High data-rate signals are therefore required to overcome pin/bumps limitations. Second, the space available in the immediate proximity of the chip is inherently limited by cost and fabrication complexity. The high data-rate signals must therefore overcome significant distances to reach the most distant memory modules.

A photonic solution offers a compelling alternative to meet these high bandwidth and longer communication distance requirements [327, 329, 330, 331], but have in the past been considered too expensive and complex to compete with electrical solutions. However, recent advances in the scalable manufacturing of high-bandwidth-density photonics and with the continued challenges scaling MCM technologies may be a tipping point for the insertion of photonic technologies into mainstream architectures. Energy efficient and compact chip-integrated silicon photonics optical transceivers have been demonstrated as well as "Optical pins", i.e. fiber-chip optical couplers that can be distributed around the die have similarly been shown realizable. Processors and memory can be connected to the photonic IOs through monolithic integration [332], flip-chip bonding [333], or through-silicon-vias [25, 334, 335], as illustrated in Fig. 6.1. All combined, these technologies should enable cost-effective and scalably manufacturable IO blocks offering wide bandwidths over distance up to ten meters. With ∼600-800 Gb/s per "pin", i.e. per fiber [336], and up to 100 fibers per chip, a total bandwidth of 10 TB/s (5 TB/s bi-directional) can be made available to the computing resources concentrated on a single chip (be it a CMP or a GPU). 5 TB/s bi-directional allows for instance a 10 TeraFLOPs many-core chips to be matched with ∼0.5-1.0 byte/FLOP,

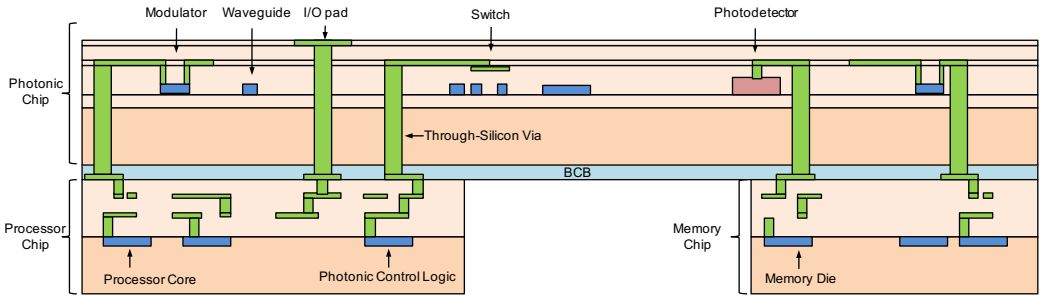


Figure 6.1: Integration of photonic and electronic chips using through-silicon-via (TSV).

a desirable metric. The resulting device is an Optically Connected Memory Module or OCMM.

These optical "pins" and transceivers offer a base level of data communication capability to match the bandwidth densities offered by 2.5D integrated electronics, but optical interconnects can also offer an extra level of re-configurability for future memory systems through optical switching. This additional re-configurability is beneficial and profoundly necessary to enable these photonic memory fabrics to be scalable. An optical switch, similarly integrated within a silicon photonic chip, can typically be inserted between the optical IOs of CMPs and OCMMs to allow bandwidth to be steered where and when it is most required. Silicon photonic switches have been demonstrated to switch Wavelength-Division Multiplexed (WDM) signals using techniques, like comb switching [202, 337, 338]. Some switches can switch in several nanoseconds [339]. A photonics-connected processor-memory system is an interdisciplinary research topic that requires knowledge of both computer architecture and optical interconnect. However, previous works are either pure simulation works (computer-architecture oriented) [324, 340, 341, 342, 343, 344] which lack experimental demonstrations of the manufacturability of the proposed systems, or are pure experimental works (optical-interconnect oriented) [332, 345, 346, 347] which demonstrate only the optical link without providing evidence of the impact on the performance of the whole system performance. In addition, most of the prior works focused on using non-reconfigurable optical interconnects (e.g. performing WDM through a single bus waveguide). To our knowledge, no published work has shown how optical switching can be leveraged in the context of a many-core multi-memory system.

The benefits brought by such reconfigurable optically connected memory systems

was investigated. The demonstrated switching time (∼15 ns) is of the same order as the transaction latency of the existing and emerging memory technologies [348], which is fast enough to enable dynamic optimization of the processor-memory interconnect at run time.

6.2 Memory-Traffic-Induced Bottlenecks

We begin by providing an overview of the memory architecture underlying most contemporary CMPs, we analyze its weaknesses and show how reconfigurable CMP-OCMMs links can benefit the architecture. Also, we present how a tunable laser combined with a WDM de-multiplexer can be used to emulate a switch, discuss the limitations of the resulting system compared to an optical spatial switch, and briefly evoke avenues to realize spatial switching while fulfilling latency requirements.

6.2.1 Overview of Memory Architecture of Contemporary CMPs

High performance commercial CMPs (both CPU- and GPU-based) have been moving towards a tiled approach consist of several identical tiles or islands that can be either compute cores, memory gateways, or in charge of specific IOs. The tiles are interconnected with a Network-on-Chip (NoC) usually in a 2D mesh or torus topology. Each memory gateway lead to a unique memory module where all the necessary memory resources are uniformly visible in a flat address space, accessible through that unique gateway. However, despite recent drastic improvements, the bandwidth (byte/s) and storage capacity (bytes) of a single memory module are by far too limited to satisfy the requirements of modern many-core processors. Moreover, such high-bandwidth memory gateways lead to major traffic hot-spots and Non-Uniform-Memory-Access (NUMA) effects once connected to a 2D-mesh organized NoC, as all the data-traffic to and from this module would be concentrated on a single spot of the NoC intersection - forcing either an over-provisioning of the NoC bandwidth, or adopting an ad-hoc NoC topology. Multiple modules are therefore connected to a CMP in parallel to provide the necessary amounts of bandwidth and capacity to the cores. For example, the Intel "Knight Landing" Xeon Phi has no less than 10 distinct gateways leading to as many independent memory modules [349]. These multiple gateways can be disseminated across the NoC, which helps to more harmoniously inject or eject traffic.

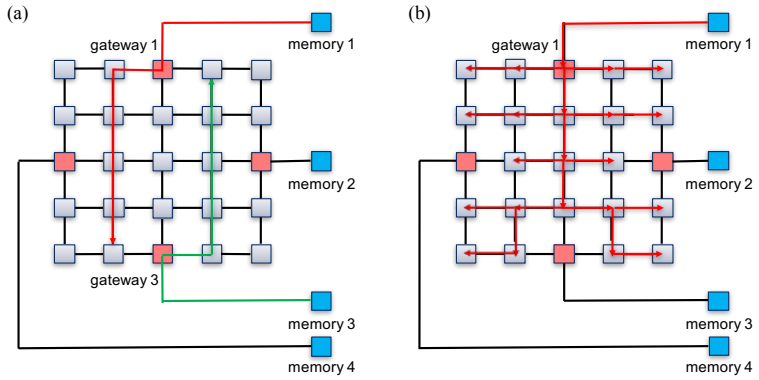


Figure 6.2: (a) Multiple cores need to communicate with one or more diametrically opposed gateways (b) The part of the NoC located around the victim gateway is saturated.

Nevertheless, even with distributed traffic injection/ejection, the system remains potentially subject to severe memory-traffic-induced NoC bottlenecks as it fails to address NUMA effects or contention due to cross-NoC traffic. We break this down into two types of bottlenecks: those arising when multiple cores need to communicate with one or more diametrically opposed gateways, and the bottlenecks caused by intensive exchanges between many cores and a unique "victim" gateway. In the first case, adversarial data-flows traversing the NoC may saturate the bisection bandwidth or create hot-spots of bandwidth contention (Fig. 6.2(a)). In the second case, the tiles located around the victim gateway can become saturated (Fig. 6.2(b)). In both cases, NoC bottlenecks prevent the "expensive" off-chip bandwidth to be fully utilized. Moreover, long journeys across the NoC also increase latency of memory requests, which is also detrimental to performance.

Adversarial situations as depicted in Fig. 6.2 can be avoided or limited by using shrewd (NUMA-aware) allocation of memory addresses across the cores a using a first-touch memory allocation policy to cause cores to exclusively communicate with the nearest memory gateway so that no excess traffic is injected onto the NoC. Realizing such a precise and always coherent allocation of memory blocks is, however, a hard task - especially when processes may be shifted around by operating systems over their lifetime. In addition, the bottlenecks can anyway be solved by over-provisioning NoC bandwidth, which is expensive both in terms of energy-efficiency and area.

To relieve the NoC from memory traffic induced bottlenecks without shifting the

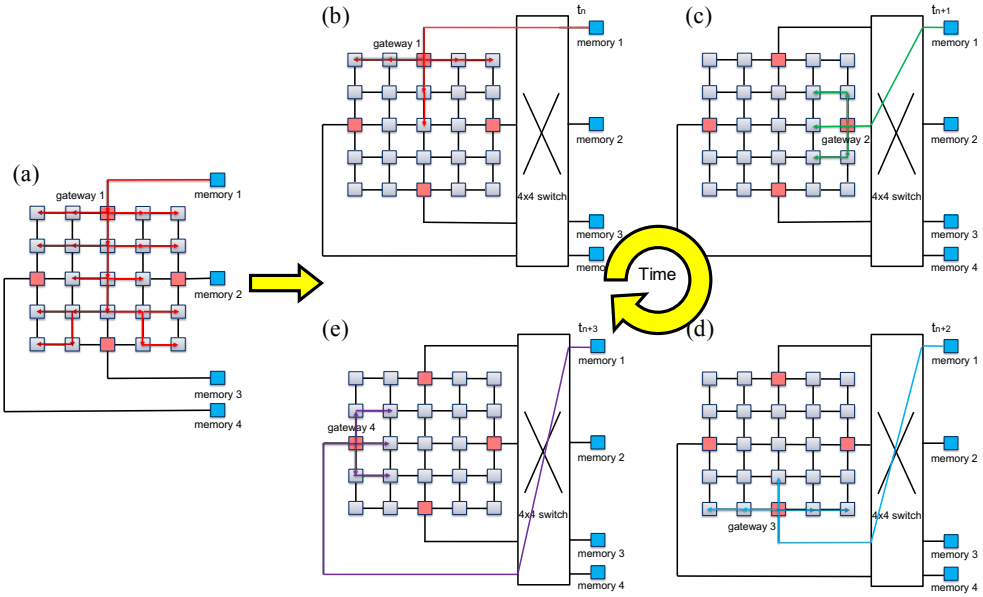


Figure 6.3: (a) 21-core 4-memory system without photonic switch (b) At time tn, traffic from memory 1 is directed to gateway 1, feeding the nearby processor cores, (c) At time tn+1, the traffic from memory 1 is re-shuffled to gateway 2, (d) At time tn+2, the traffic from memory 1 is re-shuffled to gateway 3, (e) At time tn+3, the traffic from memory 1 is re-shuffled to gateway 4.

burden onto the programmer/compiler or bandwidth over-provisioning, we here propose a novel approach of inserting an optical switch in between the gateways and the memory modules and offering multiple circuit-switched paths to shift bandwidth to where it is needed. The rationale of the concept can be described through a few examples. In situations where the memory storage available in a single module is actively solicited by numerous cores, the optical switch can be used to shuffle the mapping between gateways and the heavily solicited module (Fig. 6.3). This module's gateway can get a dedicated optical pathway directly to its destination provisioned using the optical circuit switches - permitting the memory traffic to be distributed over different sections of the NoC and thereby alleviating the bottlenecks.

The optical switch can also be leveraged to reduce the distance between cores and gateways, as shown in Fig. 6.4(a) and Fig. 6.4(b). The geometrical organization of many-core processors obliges requests to travel over a variable and potentially large number of NoC links and routers - each of which incur a delay in data transfers. In a

simple example architecture involving 4 memory gateways located in the edge middle, as depicted in Fig. 6.2 and Fig. 6.3, the hop distance between a core and a gateway can range from 1 (minimum hop counts) to 3/2n-1 (maximum hop counts) in an n-by-n mesh network, as shown in Fig. 6.4(c). In the worse-case the traffic scales with 1.5n. Fig. 6.4(c) also shows the average memory access hop count, across all cores, when each core uniquely accesses i) its nearest memory interface (perfect locality - scaling as 0.31n), equally accesses all the memory interfaces (uniform access - scaling as 0.75n), or iii) accesses its farthest memory interface (adversarial access - scaling with n). Note that there is a wide gap between perfect locality and adversarial accesses. Adversarial memory traffic asymptotically scales 3 times faster than perfectly local traffic, thus calls for 3 times larger NoC bandwidth overprovisioning to obtain the same congestion. Of course, inserting a silicon photonic switch will not transform any adversarial situation into a perfectly local one, yet the room for progression is appreciable. Our models project that we can reduce NoC bandwidth can be reduced by 1-1/1.5 = 33%.

Inserting an optical switch also reduces the hop counts by 1.5x, thus reducing request latencies. However, since optical circuit switches cannot reconfigure connectivity on a per-packet basis, request latencies might also be negatively affected if memory traffic is interrupted by the relatively coarse-grained switch reconfiguration time. To guarantee efficiency, the optical switch must be able to reconfigure itself rapidly. However, if the switching granularity is too coarse, the waiting time for the appropriate switch configuration (i.e. in Fig. 6.3, packets issued by memory 1 and destined to gateways 2, 3 and 4) starts to dominate the latency. The choice of the time separation switch adaptation is thus a fine trade-off, which we explore in the next section.

6.2.2 Emulation of Spatial Switching with Tunable Laser

As evoked in the introduction, memory links typically show bandwidth of the Terabytes/s order as CMPs or GPUs approaching 10 TFlops have ever increasing need for memory bandwidth and capacity. To obtain this kind of performance density, the full Tb/s bandwidth of a fiber is required for each link using wavelength division multiplexing (WDM). Consequently, the reconfigurable interconnect such as the one proposed here must eventually be realized with a spatial optical switch, capable of re-arranging the connectivity between N input and N output fibers.

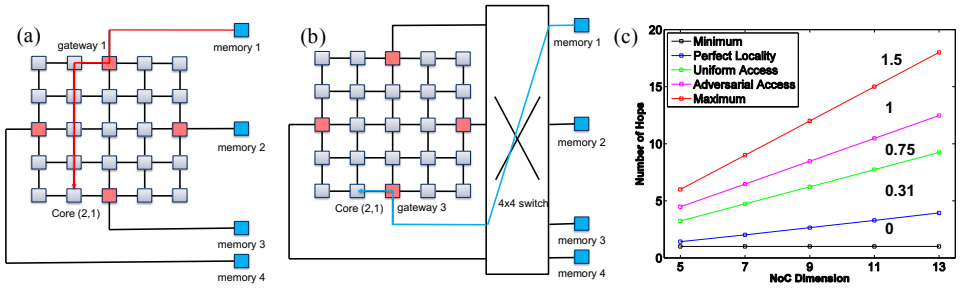


Figure 6.4: (a) A many-core multi-memory architecture using electronic interconnects. Red path: 5 hop on NoC for memory 1 to reach core (2, 1), (b) A many-core multi-memory architecture using a 4x4 switch as reconfigurable memory fabric. Green path: 1 hop for memory 1 to reach core (2, 1), (c) Number of average hops of all the cores vs. NoC dimension.

Optical spatial switches have been fabricated on silicon photonic platforms and demonstrated at the optical path level [34, 350]. However, the entire simultaneous control of the different switching elements in a dynamic environment remains challenging and has yet to be demonstrated.

To assess the feasibility of our approach, we opted for an approach where a (dynamic) spatial switch is emulated with a static WDM de-multiplexer combined with tunable lasers. Instead of directly controlling the switch to steer the optical switch to the correct output port, we change the wavelength emitted by each laser to change the optical path. By virtue of the WDM de-multiplexer, signals will be routed on distinct ports depending on their wavelength. The control mechanism is now isolated to one component per link (the laser) as opposed to direct control of the photonic switching elements, which would require many components to be controlled simultaneously to change the routing topology. Moreover, very fast tunable lasers have been demonstrated - in particular the one we leverage here [351]. The rationale of our approach can be illustrated using Fig. 6.5: in situations where the memory storage available in a single module is actively solicited by numerous cores, the tunable laser can be used to shuffle the mapping between gateways and the heavily solicited module in a round-robin fashion or a TDM manner. Note that to realize the round-robin connection of the OCMM as realized in our simulations, we only need a 1x4 functionality, therefore only one tunable laser is required.

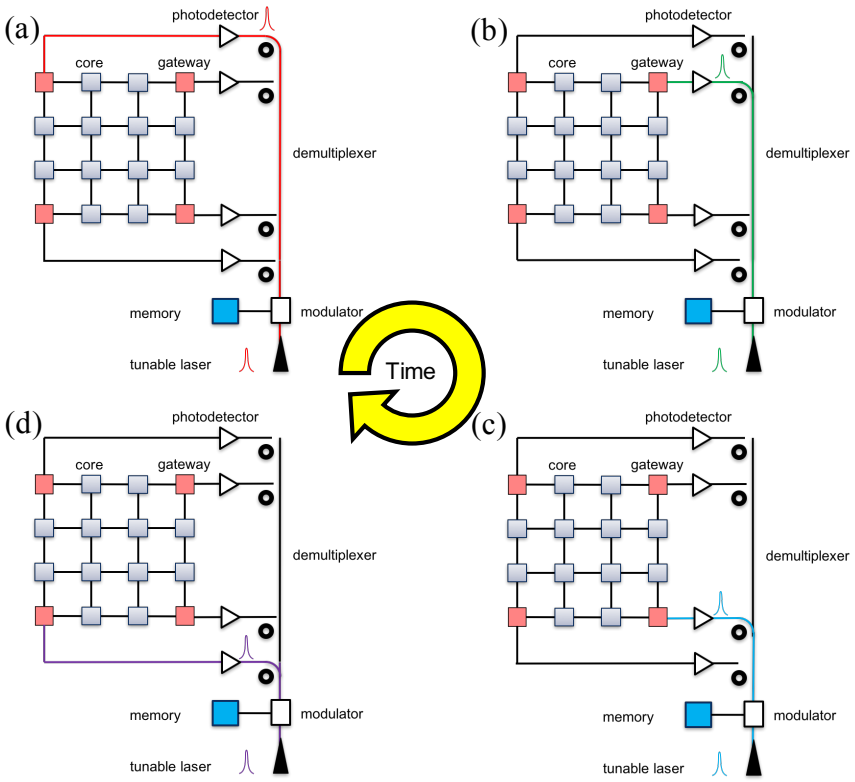


Figure 6.5: Reconfigurable photonic interconnect using a fast-tunable laser and a silicon photonic de-multiplexer (represented by the four heavy rings) (a) at time tn, traffic from memory 1 is directed to gateway 1, feeding the nearby processor cores, (b) at time tn+1, the traffic from memory 1 is re-shuffled to gateway 2, (c) at time tn+2, the traffic from memory 1 is re-shuffled to gateway 3, (d) at time tn+3, the traffic from memory 1 is re-shuffled to gateway 4. At time tn+4, the laser would be tuned back to direct the memory 1 traffic to gateway 1.

6.3 Simulation

6.3.1 Simulation Parameters and Benchmarks

We use the Structural Simulation Toolkit (SST) [352] to evaluate of our approach. The simulated NoC consists of 4 memory gateways and 21 processor cores connected in a 5x5 mesh topology (Fig. 6.6). Each memory gateway (MG) tile comprises a router and a directory controller. Every directory controller controls an external Dynamic Random-Access Memory (DRAM) clocked at 300 MHz. Each core tile comprises one SST Miranda lightweight processor, one router, 32 KB of L1 cache and 256 KB of L2

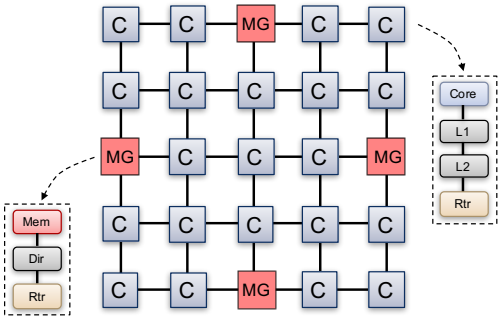


Figure 6.6: Simulated 21-core 4-memory architecture.

cache (private cache). The clock of both cores and NoC is set to 2.1 GHz to reflect a "typical" CMP use case. Considering a width of 8 Bytes for each direction, and a 25% NoC communication overhead (header, flow-control, etc.) this results in a bidirectional NoC link bandwidth of 12.6 GB/s (6 Bytes $\times$ 2.1 GHz).

We assume only the read-direction (from memory to NoC) uses silicon photonic switching functionality, while the write-direction (from NoC to memory) still uses fixed connections in order to assure memory consistency on writebacks. Miranda cores run a simple synthetic benchmark, STREAM, intended to measure sustainable memory bandwidth for simple vector kernels. To mimic a situation where a single DRAM is heavily solicited by all cores, the address space to be accessed by the STREAM benchmark is set to reside in the first memory module exclusively.

Link re-configurability is modeled in a simplified way where the most heavily accessed memory module is connected to the alternative (less congested) gateways in a round-robin fashion. A change of gateway is triggered once a predefined number of memory responses M have been sent to the current gateway, M being a parameter. The time the switch stays in the same configuration is therefore traffic dependent. For example, if M is fixed to 128, the switch remains at least for 1/300 MHz $\times$ 128 = 426 ns in the same state, which is long enough to amortize link unavailability times (resulting from re-configuration of silicon photonic switch) up to $\sim$100 ns. In general, the larger M, the longer the switch stays in the same configuration.

6.3.2 Simulation Results

We simulate two different cases. The first one is called fixed memory injection case, in which both read-direction and write-direction adopt fixed memory-to-memory-gateway

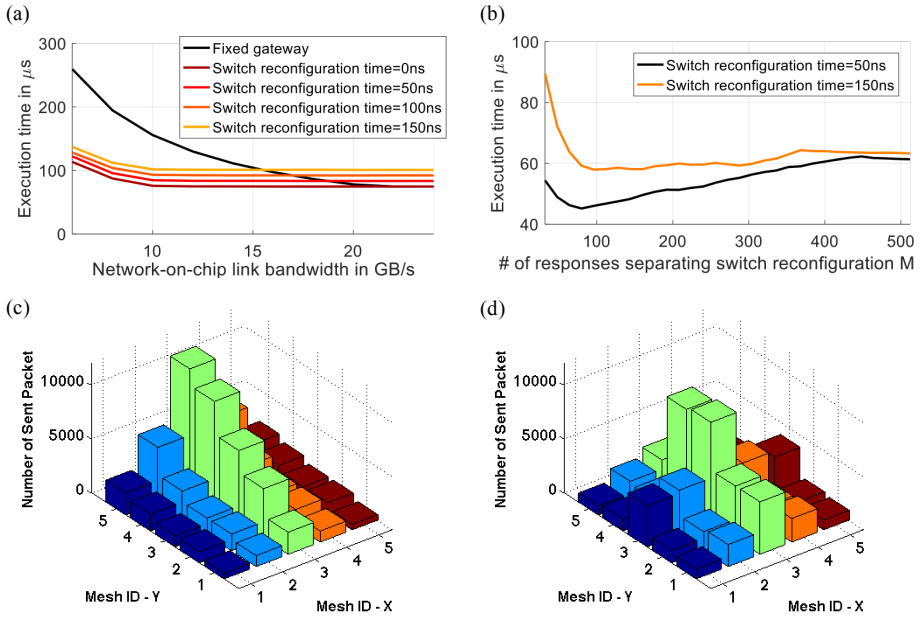


Figure 6.7: (a) Execution time of stream benchmark under fixed or TDM-switched memory connection modes, (b) Performance impact of the M parameter, which defines the number of packets between two optical reconfigurations, (c) Number of sent packet of 25 routers in mesh topology under fixed memory connection, and (d) Number of sent packet of 25 routers in mesh topology under TDM-switched memory connection.

connection. The other is called Time-Division Multiplexing (TDM)-switched case, in which only the read-direction adopts the channel switching functionality. By benchmarking TDM-switched injection case against fixed memory injection case, the performance improvement contributed by the link re-configurability can be extracted.

The execution time of STREAM kernel with fixed memory injection case or TDM-switched injection case is shown in Fig. 6.7(a). We observe that the TDM-switched injection achieves lower execution time than the fixed injection when NoC bandwidth is available in limited amounts, i.e. inferior to 15.5 GB/s (equivalent to 10 Bytes width). This is expected since the NoC traffic is linearly reduced by the reduced number of hops, which enables the architecture to tolerate more traffic before reaching the congestion point.

The insertion of an optical switch allows a substantial down-grading of the NoC bandwidth to reach the same performance level. For example, in the TDM time = 0 ns case, the NoC link bandwidth required to execute the benchmark in less than 75 μs

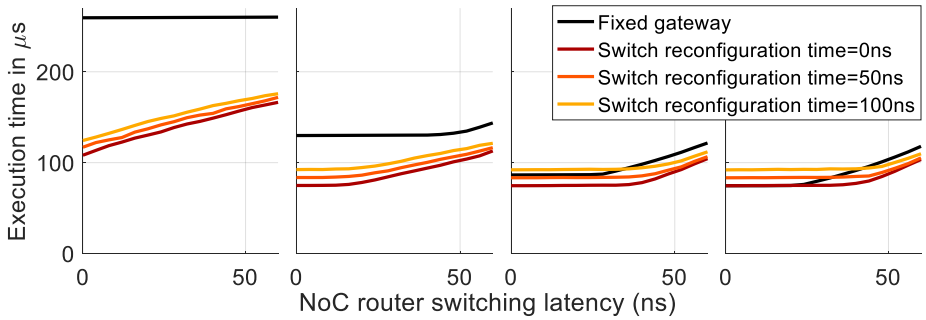


Figure 6.8: (a)-(d) Execution time of stream benchmark when changing the NoC switching latency (input/output NoC latency) with a 4 GB/s, 12 GB/s, 20 GB/s, and 24 GB/s NoC bandwidth.

is 12 GB/s, whereas 22 GB/s of NoC link bandwidth is required to achieve the same performance in the fixed case (thereby enabling a 45% reduction in bandwidth over-provisioning for the NoC). Fig. 6.7(c)-(d) compares the cumulated load offered to the 25 routers during the simulation. The impact of the optical switch on the load distribution appears clearly. Fig. 6.7(b) illustrates the performance impact of the M parameter, which dictates the frequency of switching occurrences. The NoC bandwidth is fixed to 12 GB/s. As expected, the parameter M is subject to a trade-off between frequent reconfiguration leading to efficient distribution of traffic across gateways, but important unavailability time (M small), and sporadic reconfigurations limiting unavailability but yielding lower benefits in terms of load distribution (large M). We also note that M should be selected taking the switch reconfiguration time into consideration.

Fig. 6.8(a)-(d) show the execution time of STREAM benchmark when changing the NoC switching latency (input/output NoC latency) with a 6 GB/s, 12 GB/s, 18 GB/s, and 24 GB/s NoC bandwidth. The silicon photonic switch reduces the number of hops required, and thus makes the performance less affected by potentially high per-hop latencies. Having variable injection points does not provide performance gains the 24 GB/s case, where bandwidth is abundant even for the fixed case and latencies can be hidden. In contrast, when NoC latency become significant, the reconfigurable architecture allows performance improvements, even with a relatively high switch reconfiguration time.

6.4 Experimental Demonstration

In previous section, we showed in simulation that inserting a photonic switch in between a many-core processor and several OCMMs partly alleviates the bottleneck formed by the NoC and thus increases the effective memory subsystem performance. In this Section, we investigate how such a reconfigurable interconnect can be effectively implemented to exploit the benefits of OCMMs exhibited in simulation. We prototype and experimentally evaluate our reconfigurable silicon photonic memory fabric architecture that was simulated in Section 3. To approach the tight channel switching time requirement identified in our simulation model, we leverage a tunable laser whose response time is as low as several nanoseconds to achieve rapid link re-configurability. In subsections 4.1 and 4.2, we conduct three experiments to characterize the optical link performance and demonstrate data transmission through the network.

6.4.1 Static and Dynamic Optical Link Performance

Fig. 6.9(a) shows our system testbed, which includes a tunable laser, a LiNbO3 modulator, a polarization controller, an erbium-doped fiber amplifier (EDFA), a silicon photonic 1x4 wavelength de-multiplexer, four 12.5 GHz PIN photodetectors (PDs), four trans-impedance amplifiers (TIAs) and four limiting amplifiers (LAs). Two Altera Stratix V FPGA boards are also used for control of the photonic components and to emulate the electrical components of the system (the NoC, processors, and OCMM). One 40 Gb/s quad small form-factor pluggable (QSFP) transceiver is implemented in each FPGA board using Altera's transceiver core. The electrical signal coming from the QSFP transceiver is passed through a QSFP adapter, which is plugged into the QSFP cage on the FPGA board. The QSFP adapter is used to convert the 40Gb/s QSFP transceiver into four independent 10 Gb/s transceivers, as shown in Fig. 6.9(d). Fig. 6.9(c) shows an image of the silicon photonic de-multiplexer chip. The input/output optical signals are coupled into/out of the chip through the glued fiber array. De-multiplexing is implemented using a ring resonator. Control signals of micro-ring resonators, necessary to align and stabilize the ring resonance, are applied through the landed probe.

We conducted the first experiment to verify the static optical link performance. This means that the tunable laser is fixed to one of the four wavelengths (λ_1=1548.1 nm;

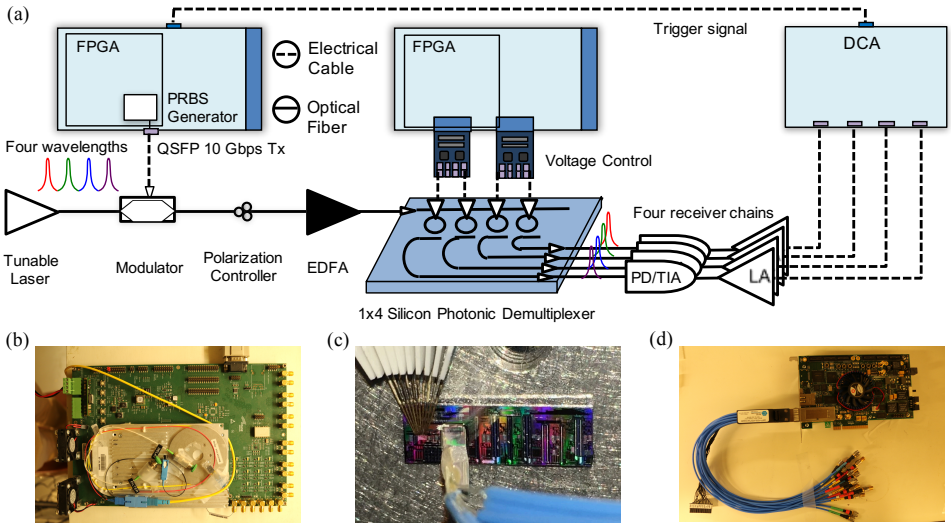


Figure 6.9: (a) Experimental setup for the characterization of the static and dynamic optical link performance, (b) Image of a fast, C-band tunable laser, (c) Chip image with probes landed and fiber array attached, and (d) Image of the Stratix V FPGA connected with QSFP cable.

λ_2=1551.3 nm; λ_3=1554.5 nm; λ_4=1557.7 nm) for the duration of the experiment, as shown in Fig. 6.9(a). A 10-Gb/s 2^{31}-1 pseudorandom binary sequence (PRBS) is first generated by the left FPGA and then transmitted through the QSFP transceivers of the FPGA boards. A RF cable (Fig. 6.9(d)) plugged into this port is used to collect the signal and route it to a RF modulator driver for amplification. The output of this driver, at the on-off keying (OOK) non-return-to-zero (NRZ) encoding, is finally applied to a broadband LiNbO3 modulator that modulates the light received from the tunable laser. The modulated data is then amplified with an EDFA to a power of 14 dBm and injected into the silicon photonic 1x4 de-multiplexer. Four micro-ring resonators in the de-multiplexer are used to selectively drop the four light channels to different output ports. On each of the four drop ports, PDs, TIAs, and LAs are used to convert the optical signals back into electrical signals. The eye diagrams (Fig. 6.10(a)) of four electrical signals are finally recorded by a digital communications analyzer (DCA). The Stratix V FPGA shown in the middle of Fig. 6.9(a) is used to tune the center wavelengths of four micro-ring resonators to the above four wavelengths, using integrated heaters through two digital-to-analog converter (DAC) daughter cards. The four micro-ring resonators of the de-multiplexer were designed far away from each other ($>$ 300 μm). So, the

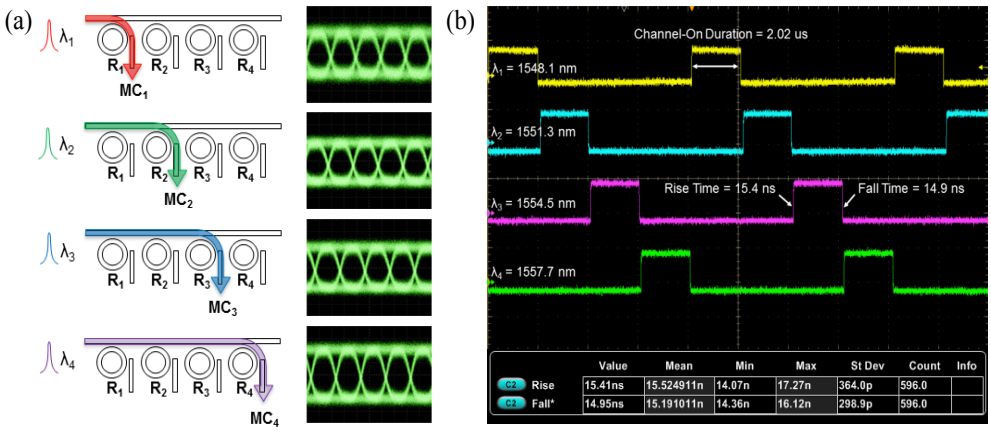


Figure 6.10: (a) Measured eye diagram, and (b) Experimental demonstration of time-sequenced switching diagrams with a channel switching time of 15 ns.

thermal crosstalk between the adjacent micro-ring resonators is very small. In the beginning of the experiment, we manually tuned the voltages of the integrated heaters to align the wavelengths of the micro-ring resonators to the desired wavelengths. This step is necessary because we need to compensate the fabrication variations. During the experiment, we did not observe any obvious wavelength drifts. Thus, the thermal stabilization is not required for our experiment. More advanced thermal stabilization techniques can be used to replace the manual adjustment [353, 354, 355].

After assessing transmission in a static configuration, we verified the dynamic reconfigurability of the optical link. In this experiment, the tunable laser is programmed to emit light during 2.02 μs onto four wavelengths successively, in a round-robin fashion. The experimental setup is the same as shown in Fig. 6.9(a). Fig. 6.10(a) show the eye diagram of four optical wavelengths routed in four different static configurations of the 1x4 Silicon photonic de-multiplexer. Clear and open eyes indicate that the physical layer of the network is capable of error-free data transmission (bit error rate $< 10^{-12}$). Fig. 6.10(b) illustrates the measured responses at the four drop ports of the Silicon photonic de-multiplexer using a four-channel oscilloscope. The figure shows that the four channels are turned on/off in a round-robin fashion because of the switching of the tunable laser. The measured switching time (defined by the rise/fall time) of the signal recovered at the output is 15 ns.

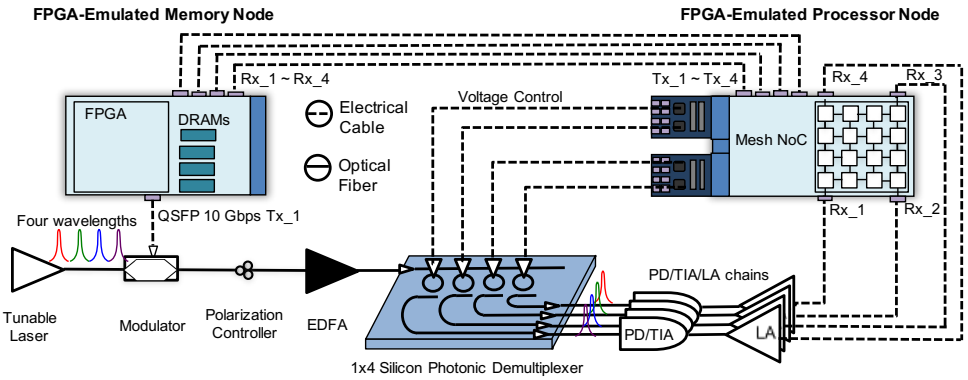


Figure 6.11: Experimental setup for data transmission demonstration.

6.4.2 Data Transmission

We performed the last experiment to show data transmission between two FPGAs using the proposed reconfigurable optical link. Fig. 6.11 shows the implemented experimental setup. Two Altera Stratix V FPGAs with 4x10-Gb/s QSFP transceivers are used to emulate the processor side and OCMM side, respectively. The processor chip is emulated by a 4x4 mesh NoC generated and synthesized for the FPGA using OpenSoC Fabric [356], a NoC hardware generator based on the CHISEL Hardware Description Language (HDL). The generated NoC contains 16 tiles. Four of them are memory gateway tiles, which locate at the four corners of the mesh and are connected directly to the output of the four LAs. Other tiles are dummies just used as sinks for incoming packets. The OpenSoC NoC allows the flits to be routed from any memory gateway tiles to any destination tiles and vice-versa. The flits received from the memory are collected at the four memory gateway tiles of the OpenSoC fabric, packaged as payload by the synthesized routers, and routed with their respective destination tiles. The memory requests, which include the information of destination tile number, initial data address, and data length, are generated by a simple memory request generator implemented in the processor node. To emulate the memory node, we use the Altera's provided memory controller to read/write data from/into the four on-board SDRAMs, through a 72-bit wide bus.

In memory-to-processor direction, the reconfigurable silicon photonic link is implemented as in the two previous experiments. Depending on the different wavelengths of the tunable laser, an optical link is established between one Tx port of the QSFP

transceiver in memory node to one of the four Rx ports of the QSFP transceiver in processor node, each port being routed to the four memory tiles. In processor-to-memory direction, four RF cables are used to connect the four Tx ports of the QSFP transceiver in processor node to the Rx ports of the QSFP transceiver in memory node.

The experimental procedure is as follows: (i) the micro-ring resonators of the silicon photonic de-multiplexer are tuned to the designated wavelengths by applying proper biasing control voltages through the DACs of right FPGA, (ii) tunable laser is programmed to switch among four wavelengths in a round-robin fashion starting from wavelength (λ_1), (iii) right FPGA monitors the output power from the four PD/TIA/LA chains. When the right FPGA detects high voltage at Rx1, it recognizes the tunable laser is switched to wavelength (λ_1) and then sends a packet with the SYN (or synchronization) message through Tx1 to the left FPGA to establish a new connection, (iv) left FPGA returns a packet with the SYN and ACK (or acknowledgement) message through its own Tx1, (v) the right FPGA returns a packet with just the ACK message, notifying the left FPGA that the connection has been established using wavelength λ_1, (vi) the memory request generator in the right FPGA sends a read command with the data initial address, data size information, and destination core number to the left FPGA, (vii) the left FPGA reads the requested data from the DRAMs (viii) the requested memory data is sent on the QSFP transceiver's 1st channel toward the optical interconnect; if the requested data size is larger than the maximum data size that can be transferred during the period when laser stays in wavelength (λ_1), the data is buffered and transferred when laser is switched to the next wavelength and a new connection is established, (ix) the data packet is dropped by de-multiplexer at different PD/TIA/LA chains which connect to the different memory gateway tiles, and (x) the data packet is routed to the correct tile through the OpenSoC switch fabric.

It is worth noting that steps (iii)-(v) is a three-way handshake [357] process that not only helps establishing a full-duplex connection between two FPGAs, but more importantly allows the transceivers to complete clock and data recovery (CDR). In this experiment, every time laser tunes its wavelength, the related Rx/Tx pair at the processor node is activated, while others go to idle state. The newly-activated Rx/Tx pair at the processor node needs to perform this three-way hand shake with the counterparts at the memory node to complete the CDR. So, even though the laser is keep switching its wavelengths, the data read from memory is only transmitted when the CDR

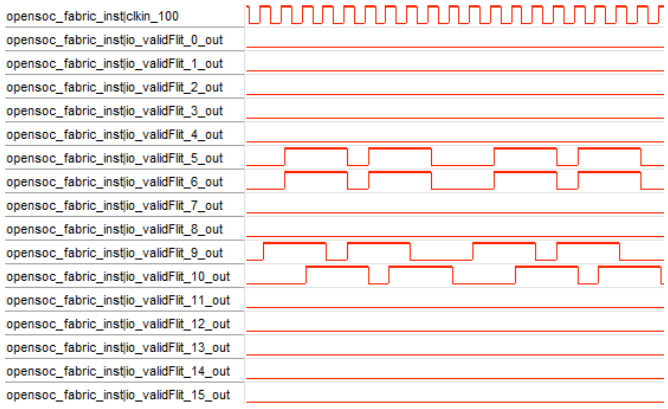


Figure 6.12: OpenSoC switch fabric outputs showing four cores simultaneously receiving memory data from four memory interfaces.

is completed and the links support error-free transmission. Note that any handshake process/packet transmission must be performed when the laser gets stable at one of the four wavelengths and stopped during the period when the laser is switching (about 15 ns). This synchronization between laser and the two FPGAs is achieved during steps (ii)-(iii).

Fig. 6.12 depicts the output timing diagram captured using the SignalTap tool offered by Altera's Quartus-II development environment. The packets are routed to four different processor tiles through the mesh NoC. The top-most signal is a 100 MHz clock signal that drives the OpenSoC fabric. The other 16 signals are the output valid flags indicating that a packet is being passed by a router to its corresponding core. Received Flits from four different memory gateways are routed to their respective output ports (5, 6, 9, 10) successfully, while other ports remain "quiet".

In sum, we prototyped a reconfigurable silicon photonic interconnect using a tunable laser, a silicon photonic de-multiplexer, and two FPGAs. We characterized optical link performance and demonstrated error-free transmission and fast link reconfiguration. The demonstrated optical interconnect shows a nanosecond-level (15 ns) channel switching latency, which makes our proposed scheme both practical and performant.

6.5 Conclusion

In this study, we show that runtime optical re-configurability implemented with silicon photonic switches can be used to offload network-on-chips from memory traffic. This

enables a reduction of area and power budgets allocated to the network-on-chip, and ensures an optimal utilization of off-chip memory links. Simulation results indicate that to achieve significant speedup of performance, the channel reconfiguration time must be in the tens of nanoseconds regime, otherwise, the channel reconfiguration overhead will slow down the system performance. To approach this tight channel switching time requirement, we prototype a reconfigurable silicon photonic interconnect using a fast-tunable laser and a silicon photonic de-multiplexer. The demonstrated optical interconnect shows a nanosecond-level (15 ns) channel switching latency, which makes such a design both practical and performant. We believe that our proposed silicon photonic interconnect can be a promising solution to address the memory access issues in the many-core era.

Chapter 7

Summary and Conclusion

7.1 Summary of Contributions

This work demonstrated a new design and optimization methodology for silicon photonic devices. The use of particle swarm optimization in conjunction with 3D FDTD simulation is a powerful tool to design small-footprint and high-performance silicon photonic devices. The polarization rotator and 90° optical hybrid are two good examples showing how this method can be used to design outstanding devices.

Furthermore, this work demonstrated a polarization-insensitive short-reach WDM receiver and a high-performance C-band tunable laser for coherent transmission. The two seemingly unrelated works address equally important issues faced by polarization-diversity and phase-diversity communication systems, respectively.

Lastly, this work demonstrated an Optically Connected Memory Module (OCMM) which offers a new nanophotonics-based approach for handling bandwidth bottlenecks. At high bandwidth densities, the Network-on-Chip (NoC) becomes the primary bottleneck of the architecture, so the memory modules are organized in a re- configurable nanophotonic interconnect fabric that adapts to memory access patterns.

7.2 Recommendations for Future Work

On the topic of silicon photonic device design and optimization, especially the geometric optimization of passive silicon photonic devices, the following research ideas are suggested:

- Utilize particle swarm optimization to design novel passive silicon photonic devices, like metastructures [358].
- Investigate other evolutionary algorithms, like genetic algorithm [218].
- Investigate more counter-intuitive inverse design algorithms, like directory binary search algorithm [224, 225, 226].
- Apply the evolutionary computation/inverse design algorithms to the design of active silicon photonics, like the optimization of the p-i-n junction of traveling-wave Mach-Zehnder modulator.
- Implement a distributed optimization algorithm, which can better utilize the increasingly widespread cloud computing infrastructures.

On the topic of silicon photonic lasers and transceivers, the following research ideas are suggested:

- Optimize the coupling loss of the III/V chip and the silicon photonic chip to maximize the output power and reduce the threshold current.
- Optimize the geometric and gain profile of the III-V chip to achieve higher gain across the entire C-band.
- Develop the control algorithm to avoid mode-hopping during laser operation.
- Optimize a cascaded Mach-Zehnder demultiplexer to achieve lower loss, thus higher receiver sensitivity.

On the topic of reconfigurable optical interconnects, the following research ideas are suggested:

- Implement the benchmarks in an FPGA.
- Implement an ultrafast silicon-photonic switch fabric that can switch in nanoseconds.
- Investigate the reconfigurable optical interconnects for the next-generation memory modules, like Hybrid Memory Cube (HMC), High Bandwidth Memory (HBM).

7.3 Final Remarks

It is well established that silicon photonics can leverage the mature CMOS-style design, fabrication and test infrastructure to achieve high chip reproducibility and uniformity at low cost. After two decades of active research and development, silicon photonics is transferring from the laboratory to marketplace.

Optical transceivers for the data center and telecommunication alike are very promising application areas for silicon photonics. However, to successfully build and bring a silicon-photonic transceiver product to the market is not an easy task. It requires a team of multi-disciplinary experts to address a wide range of issues from design through fabrication, testing and analysis.

Within this context, the device-level innovation and system-level analysis, such as demonstrated in this dissertation, will continue to grow in importance.

References

[1] Martin Hilbert and Priscila López. **The worlds technological capacity to store, communicate, and compute information**. *Science*, **332**(6025):60–65, 2011. 1

[2] Cisco Visual Networking. **The zettabyte era–trends and analysis**. *Cisco white paper*, 2015. 1

[3] Robert W Tkach. **Scaling optical communications for the next decade and beyond**. *Bell Labs Technical Journal*, **14**(4):3–9, 2010. 1, 30

[4] Daryl Inniss and Roy Rubenstein. *Silicon Photonics: Fueling the Next Information Revolution*. Morgan Kaufmann, 2016. 1

[5] Mehdi Asghari and Ashok V Krishnamoorthy. **Silicon photonics: Energy-efficient communication**. *Nature Photonics*, **5**(5):268–270, 2011. 1, 52

[6] Andrew Rickman. **The commercialization of silicon photonics**. *Nature Photonics*, **8**(8):579, 2014. 1

[7] RA Soref and JP Lorenzo. **Single-crystal silicon: a new material for 1.3 and 1.6 μm integrated-optical components**. *Electronics Letters*, **21**(21):953–954, 1985. 1

[8] Graham T Reed, William Robert Headley, and CE Jason Png. **Silicon photonics: The early years**. In *Optoelectronic Integration on Silicon II*, **5730**, pages 1–19. International Society for Optics and Photonics, 2005. 1

[9] Richard Soref. **The past, present, and future of silicon photonics**. *IEEE Journal of Selected Topics in Quantum Electronics*, **12**(6):1678–1687, 2006. 1

[10] Richard A Soref, Joachim Schmidtchen, and Klaus Petermann. **Large single-mode rib waveguides in GeSi-Si and Si-on-SiO/sub 2**. *IEEE Journal of Quantum Electronics*, **27**(8):1971–1974, 1991. 1

[11] AG Rickman, GT Reed, and Fereydoon Namavar. **Silicon-on-insulator optical rib waveguide loss and mode characteristics**. *Journal of Lightwave Technology*, **12**(10):1771–1776, 1994. 1

[12] Gerhard Abstreiter. **Engineering the future of electronics**. *Physics World*, **5**(3):36, 1992. 2

[13] Richard A Soref. **Silicon-based optoelectronics**. *Proceedings of the IEEE*, **81**(12):1687–1706, 1993. v, 2

[14] Richard A Soref and Brian R Bennett. **Kramers-Kronig analysis of electro-optical switching in silicon**. In *Integrated Optical Circuit Engineering IV*, **704**, pages 32–38. International Society for Optics and Photonics, 1987. 2

[15] Graham T Reed, David J Thomson, Frederic Y Gardes, Youfang Hu, Jean-Marc Fedeli, and Goran Z Mashanovich. **High-speed carrier-depletion silicon Mach-Zehnder optical modulators with lateral PN junctions**. *Frontiers in Physics*, **2**:77, 2014. 2

[16] D Marris-Morini, L Virot, C Baudot, J-M Fédéli, G Rasigade, D Perez-Galacho, J-M Hartmann, S Olivier, P Brindel, P Crozat, et al. **A 40 Gbit/s optical link on a 300-mm silicon platform**. *Optics Express*, **22**(6):6674–6679, 2014. 2

[17] H Temkin, TP Pearsall, JC Bean, RA Logan, and S Luryi. **Ge x Si1- x strained-layer superlattice waveguide photodetectors operating near 1.3 μm**. *Applied Physics Letters*, **48**(15):963–965, 1986. 2

[18] Jifeng Liu, Douglas D Cannon, Kazumi Wada, Yasuhiko Ishikawa, Samerkhae Jongthammanurak, David T Danielson, Jurgen Michel, and Lionel C Kimerling. **Tensile strained Ge p-i-n photodetectors on Si platform for C and L band telecommunications**. *Applied Physics Letters*, **87**(1):011110, 2005. 2

[19] Dazeng Feng, Jonathan Luff, Shashank Jatar, and Medhi Asghari. **Micron-scale silicon photonic devices and circuits**. In *Optical Fiber Communication Conference*, pages Th4C–1. Optical Society of America, 2014. 2, 3

[20] Laurent Vivien, Andreas Polzer, Delphine Marris-Morini, Johann Osmond, Jean Michel Hartmann, Paul Crozat, Eric Cassan, Christophe Kopp, Horst Zimmermann, and Jean Marc Fédéli. **Zero-bias 40Gbit/s germanium waveguide photodetector on silicon**. *Optics Express*, **20**(2):1096–1101, 2012. 2, 9

[21] Qianfan Xu, Bradley Schmidt, Sameer Pradhan, and Michal Lipson. **Micrometre-scale silicon electro-optic modulator**. *Nature*, **435**(7040):325, 2005. 2

[22] Qianfan Xu, Sasikanth Manipatruni, Brad Schmidt, Jagat Shakya, and Michal Lipson. **12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators**. *Optics Express*, **15**(2):430–436, 2007. 2

[23] DTH Tan, A Grieco, and Y Fainman. **Towards 100 channel dense wavelength division multiplexing with 100GHz spacing on silicon**. *Optics Express*, **22**(9):10408–10415, 2014. 2

[24] Yasushi Takahashi, Takashi Asano, Daiki Yamashita, and Susumu Noda. **Ultra-compact 32-channel drop filter with 100 GHz spacing**. *Optics Express*, **22**(4):4692–4698, 2014. 2

[25] Christophe Kopp, Stephane Bernabe, Badhise Ben Bakir, Jean-Marc Fedeli, Regis Orobtchouk, Franz Schrank, Henri Porte, Lars Zimmermann, and Tolga Tekin. **Silicon photonic circuits: on-CMOS integration, fiber optical coupling, and packaging**. *IEEE Journal of Selected Topics in Quantum Electronics*, **17**(3):498–509, 2011. 2, 11, 70

REFERENCES

[26] Diedrik Vermeulen, S Selvaraja, Pl Verheyen, G Lepage, W Bogaerts, P Absil, D Van Thourhout, and G Roelkens. **High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible silicon-on-insulator platform**. *Optics Express*, **18**(17):18278–18283, 2010. 2

[27] Wissem Sfar Zaoui, Andreas Kunze, Wolfgang Vogel, Manfred Berroth, Jörg Butschke, Florian Letzkus, and Joachim Burghartz. **Bridging the gap between optical fibers and silicon photonic integrated circuits**. *Optics Express*, **22**(2):1277–1286, 2014. 2

[28] B Ben Bakir, A Vazquez De Gyves, R Orobtchouk, P Lyan, C Porzier, A Roman, and J-M Fedeli. **Low-Loss (<1 dB) and Polarization-Insensitive Edge Fiber Couplers Fabricated on 200-mm Silicon-on-Insulator Wafers**. *IEEE Photonics Technology Letters*, **22**(11):739–741, 2010. 2

[29] Attila Mekis, Steffen Gloeckner, Gianlorenzo Masini, Adithyaram Narasimha, Thierry Pinguet, Subal Sahni, and Peter De Dobbelaere. **A grating-coupler-enabled CMOS photonics platform**. *IEEE Journal of Selected Topics in Quantum Electronics*, **17**(3):597–608, 2011. 2

[30] Ansheng Liu, Ling Liao, Doron Rubin, Hat Nguyen, Berkehan Ciftcioglu, Yoel Chetrit, Nahum Izhaky, and Mario Paniccia. **High-speed optical modulation based on carrier depletion in a silicon waveguide**. *Optics Express*, **15**(2):660–668, 2007. 2

[31] Nicholas C Harris, Yangjin Ma, Jacob Mower, Tom Baehr-Jones, Dirk Englund, Michael Hochberg, and Christophe Galland. **Efficient, compact and low loss thermo-optic phase shifter in silicon**. *Optics Express*, **22**(9):10487–10493, 2014. 2

[32] Andrew W Poon, Xianshu Luo, Fang Xu, and Hui Chen. **Cascaded microresonator-based matrix switch for silicon on-chip optical interconnection**. *Proceedings of the IEEE*, **97**(7):1216–1238, 2009. 2

[33] Long Chen and Young-kai Chen. **Compact, low-loss and low-power 8× 8 broadband silicon optical switch**. *Optics Express*, **20**(17):18977–18985, 2012. 2

[34] Benjamin G Lee, Alexander V Rylyakov, William MJ Green, Solomon Assefa, Christian W Baks, Renato Rimolo-Donadio, Daniel M Kuchta, Marwan H Khater, Tymon Barwicz, Carol Reinholm, et al. **Monolithic silicon integration of scaled photonic switch fabrics, CMOS logic, and device driver circuits**. *Journal of Lightwave Technology*, **32**(4):743–751, 2014. 2, 76

[35] Nicolás Sherwood-Droz, Howard Wang, Long Chen, Benjamin G Lee, Aleksandr Biberman, Keren Bergman, and Michal Lipson. **Optical 4× 4 hitless silicon router for optical networks-on-chip (NoC)**. *Optics Express*, **16**(20):15915–15922, 2008. 2

[36] Francesco Bonaccorso, Z Sun, Ta Hasan, and AC Ferrari. **Graphene photonics and optoelectronics**. *Nature Photonics*, **4**(9):611, 2010. 2

[37] Konstantin S Novoselov, VI Fal, L Colombo, PR Gellert, MG Schwab, K Kim, et al. **A roadmap for graphene**. *Nature*, **490**(7419):192, 2012. 2

[38] Ming Liu, Xiaobo Yin, Erick Ulin-Avila, Baisong Geng, Thomas Zentgraf, Long Ju, Feng Wang, and Xiang Zhang. **A graphene-based broadband optical modulator**. *Nature*, **474**(7349):64, 2011. 2, 9

[39] Qiaoliang Bao and Kian Ping Loh. **Graphene photonics, plasmonics, and broadband optoelectronic devices**. *ACS nano*, **6**(5):3677–3694, 2012. 2

[40] FHL Koppens, T Mueller, Ph Avouris, AC Ferrari, MS Vitiello, and M Polini. **Photodetectors based on graphene, other two-dimensional materials and hybrid systems**. *Nature Nanotechnology*, **9**(10):780, 2014. 2

[41] Christopher T Phare, Yoon-Ho Daniel Lee, Jaime Cardenas, and Michal Lipson. **Graphene electro-optic modulator with 30 GHz bandwidth**. *Nature Photonics*, **9**(8):511, 2015. 2, 9

[42] Wesley D Sacher, Ying Huang, Guo-Qiang Lo, and Joyce KS Poon. **Multilayer silicon nitride-on-silicon integrated photonic platforms and devices**. *Journal of Lightwave Technology*, **33**(4):901–910, 2015. 3

[43] Kuanping Shang, Shibnath Pathak, Binbin Guan, Guangyao Liu, and SJB Yoo. **Low-loss compact multilayer silicon nitride platform for 3D photonic integrated circuits**. *Optics Express*, **23**(16):21334–21342, 2015. 3

[44] Di Liang and John E Bowers. **Recent progress in lasers on silicon**. *Nature Photonics*, **4**(8):511, 2010. 3

[45] Alexander W Fang, Hyundai Park, Oded Cohen, Richard Jones, Mario J Paniccia, and John E Bowers. **Electrically pumped hybrid AlGaInAs-silicon evanescent laser**. *Optics Express*, **14**(20):9203–9210, 2006. 3, 52

[46] Brian R Koch, Erik J Norberg, Byungchae Kim, John Hutchinson, Jae-Hyuk Shin, Gregory Fish, and Alexander Fang. **Integrated silicon photonic laser sources for telecom and datacom**. In *National Fiber Optic Engineers Conference*, pages PDP5C–8. Optical Society of America, 2013. 3

[47] Hyundai Park, Alexander W Fang, Oded Cohen, Richard Jones, Mario J Paniccia, and John E Bowers. **A hybrid AlGaInAs–silicon evanescent amplifier**. *IEEE Photonics Technology Letters*, **19**(4):230–232, 2007. 3

[48] Mark A Foster, Amy C Turner, Jay E Sharping, Bradley S Schmidt, Michal Lipson, and Alexander L Gaeta. **Broad-band optical parametric gain on a silicon photonic chip**. *Nature*, **441**(7096):960, 2006. 3

[49] Martijn JR Heck, Jared F Bauters, Michael L Davenport, Jonathan K Doylend, Siddharth Jain, Géza Kurczveil, Sudharsanan Srinivasan, Yongbo Tang, and John E Bowers. **Hybrid silicon photonic integrated circuit technology**. *IEEE Journal of Selected Topics in Quantum Electronics*, **19**(4):6100117–6100117, 2013. 3, 12

[50] Lei Bi, Juejun Hu, Peng Jiang, Dong Hun Kim, Gerald F Dionne, Lionel C Kimerling, and CA Ross. **On-chip optical isolation in monolithically integrated non-reciprocal optical resonators**. *Nature Photonics*, **5**(12):758, 2011. 3

[51] Yuya Shoji and Tetsuya Mizumoto. **Magneto-optical non-reciprocal devices in silicon photonics**. *Science and Technology of Advanced Materials*, **15**(1):014602, 2014. 3

[52] Ming-Chun Tien, Tetsuya Mizumoto, Paolo Pintus, Herbert Kromer, and John E Bowers. **Silicon ring isolators with bonded nonreciprocal magneto-optic garnets**. *Optics Express*, **19**(12):11740–11745, 2011. 3

[53] Peter De Dobbelaere, Sherif Abdalla, Steffen Gloeckner, Michael Mack, Gianlorenzo Masini, Attila Mekis, Thierry Pinguet, Subal Sahni, Adithyaram Narasimha, Drew Guckenberger, et al. **Si photonics based high-speed optical transceivers**. In *European Conference and Exhibition on Optical Communication*, pages We–1. Optical Society of America, 2012. 3

[54] T Pinguet, B Analui, E Balmater, D Guckenberger, M Harrison, R Koumans, D Kucharski, Y Liang, G Masini, A Mekis, et al. **Monolithically integrated high-speed CMOS photonic transceivers**. In *Group IV Photonics, 2008 5th IEEE International Conference on*, pages 362–364. IEEE, 2008. 3

[55] Peter De Dobbelaere, G Armijo, J Balardeta, B Chase, Y Chi, A Dahl, Y De Koninck, S Denton, M Eker, S Fathpour, et al. **Silicon-photonics-based optical transceivers for high-speed interconnect applications**. In *Next-Generation Optical Networks for Data Centers and Short-Reach Links III*, **9775**, page 977503. International Society for Optics and Photonics, 2016. v, 3, 4

[56] Mehdi Asghari. **Silicon photonics: a low cost integration platform for datacom and telecom applications**. In *National Fiber Optic Engineers Conference*, page NThA4. Optical Society of America, 2008. 3

[57] Sean Koehl, Ansheng Liu, and Mario Paniccia. **Integrated silicon photonics: Harnessing the data explosion**. *Optics and Photonics News*, **22**(3):24–29, 2011. 3

[58] Ansheng Liu, Ling Liao, Yoel Chetrit, Juthika Basak, Hat Nguyen, Doron Rubin, and Mario Paniccia. **200 Gbps photonic integrated chip on silicon platform**. In *Group IV Photonics, 2008 5th IEEE International Conference on*, pages 368–370. IEEE, 2008. 3

[59] Xin Chen, Scott R Bickham, Hai-Feng Liu, Olufemi I Dosunmu, Jason E Hurley, and Ming-Jun Li. **25 Gb/s transmission over 820 m of MMF using a multimode launch from an integrated silicon photonics transceiver**. *Optics Express*, **22**(2):2070–2077, 2014. 3

[60] Biljana Milivojevic, Christian Raabe, Anujit Shastri, Mark Webster, Peter Metz, Sanjay Sunder, Bill Chattin, Stefan Wiese, Bipin Dama, and Kal Shastri. **112Gb/s DP-QPSK transmission over 2427km SSMF using small-size silicon photonic IQ modulator and low-power CMOS driver**. In *Optical Fiber Communication Conference*, pages OTh1D–1. Optical Society of America, 2013. 3, 5, 52

[61] M Mazzini, M Traverso, M Webster, C Muzio, S Anderson, P Sun, D Siadat, D Conti, A Cervasio, S Pfnuer, et al. **25GBaud PAM-4 error free transmission over both single mode fiber and multimode fiber in a QSFP form factor based on silicon photonics**. In *Optical Fiber Communications Conference and Exhibition (OFC), 2015*, pages 1–3. IEEE, 2015. 3, 4, 52

[62] Christopher R Doerr, Long Chen, Diedrik Vermeulen, Torben Nielsen, Saeid Azemati, Scott Stulz, Greg McBrien, Xiao-Ming Xu, Benny Mikkelsen, Mehrdad Givehchi, et al. **Single-chip silicon photonics 100-Gb/s coherent transceiver**. In *Optical Fiber Communication Conference*, pages Th5C–1. Optical Society of America, 2014. 3, 52

[63] E Mounier and J.-L. Malinge. **Silicon Photonics 2018 Market & Technology report**. *Yole Développement Market Report*, 2018. v, 3

[64] Kevin Bédard, Alexandre D Simard, Benoit Filion, Yves Painchaud, Leslie A Rusch, and Sophie LaRochelle. **Dual phase-shift Bragg grating silicon photonic modulator operating up to 60 Gb/s**. *Optics Express*, **24**(3):2413–2419, 2016. 4

[65] Daniel Mahgerefteh, Craig Thompson, Chris Cole, Gilles Denoyer, Thelinh Nguyen, Ilya Lyubomirsky, Chris Kocot, and Jim Tatum. **Techno-economic comparison of silicon photonics and multimode VCSELs**. *Journal of Lightwave Technology*, **34**(2):233–242, 2016. 4

[66] Yurii A Vlasov. **Silicon CMOS-integrated nano-photonics for computer and data communications beyond 100G**. *IEEE Communications Magazine*, **50**(2), 2012. 4

[67] Tam N Huynh, Nicolas Dupuis, Renato Rimolo-Donadio, Jonathan E Proesel, Doug M Gill, Christian W Baks, Alexander V Rylyakov, Clint L Schow, William MJ Green, and Benjamin G Lee. **Flexible transmitter employing Silicon-segmented Mach–Zehnder modulator with 32-nm CMOS distributed driver**. *Journal of Lightwave Technology*, **34**(22):5129–5136, 2016. 4

[68] Yu Li, Yu Zhang, Lei Zhang, and Andrew W Poon. **Silicon and hybrid silicon photonic devices for intra-datacenter applications: state of the art and perspectives**. *Photonics Research*, **3**(5):B10–B27, 2015. 4

[69] Hai-Feng Liu. **Integrated silicon photonics links for high bandwidth data transportation**. In *Optical Fiber Communication Conference*, pages Th1D–1. Optical Society of America, 2014. 4, 52

[70] Christopher Richard Doerr. **Silicon photonic integration in telecommunications**. *Frontiers in Physics*, **3**:37, 2015. 4, 52

[71] Peter J Winzer and R-J Essiambre. **Advanced optical modulation formats**. *Proceedings of the IEEE*, **94**(5):952–985, 2006. 5

[72] Koji Yamada, Tai Tsuchizawa, Hidetaka Nishi, Rai Kou, Tatsurou Hiraki, Kotaro Takeda, Hiroshi Fukuda, Yasuhiko Ishikawa, Kazumi Wada, and Tsuyoshi Yamamoto. **High-performance silicon photonics technology for telecommunications applications**. *Science and Technology of Advanced Materials*, **15**(2):024603, 2014. 5

REFERENCES

[73] Geoff Bennett, Kuang-Tsan Wu, Anuj Malik, Soumya Roy, and Ahmed Awadalla. **A review of high-speed coherent transmission technologies for long-haul DWDM transmission at 100G and beyond**. *IEEE Communications Magazine*, **52**(10):102–110, 2014. 5

[74] Kim Roberts, Sik Heng Foo, Michael Moyer, Michael Hubbard, Andrew Sinclair, Jamie Gaudette, and Charles Laperle. **High capacity transport100G and beyond**. *Journal of Lightwave Technology*, **33**(3):563–578, 2015. 5

[75] C Doerr, John Heanue, Long Chen, Ricado Aroca, Saeid Azemati, Gaz Ali, Greg McBrien, Li Chen, Binbin Guan, Hongbin Zhang, et al. **Silicon photonics coherent transceiver in a ball-grid array package**. In *Optical Fiber Communications Conference*, pages 1–3. IEEE, 2017. 5, 11, 52

[76] Long Chen, Chris Doerr, R Aroca, SY Park, JC Geyer, T Nielsen, C Rasmussen, and B Mikkelsen. **Silicon Photonics for Coherent Transmission**. In *Optical Fiber Communication Conference*, pages Th1B–1. Optical Society of America, 2016. 5

[77] CRS Fludger, ES Vercelli, G Marenco, A Della Torre, T Duthel, and T Kupfer. **1Tb/s Real-Time 4× 40 Gbaud DP-16QAM Super-Channel Using CFP2-ACO Pluggable Modules Over 625 km of Standard Fiber**. *Journal of Lightwave Technology*, **35**(4):949–954, 2017. 5, 52

[78] Po Dong, Xiang Liu, S Chandrasekhar, Lawrence L Buhl, Ricardo Aroca, and Young-Kai Chen. **Monolithic silicon photonic integrated circuits for compact 100 Gb/s coherent optical receivers and transmitters**. *IEEE Journal of Selected Topics in Quantum Electronics*, **20**(4):1–8, 2014. 5, 30, 52

[79] L. Chen, C. Doerr, R. Aroca, S. Y. Park, J. C. Geyer, T. Nielsen, C. Rasmussen, and B. Mikkelsen. **Silicon photonics for 100G-and-beyond coherent transmissions**. In *Optical Fiber Communications Conference*, pages 1–3, March 2016. v, 5

[80] Lukas Chrostowski and Michael Hochberg. *Silicon photonics design: from devices to systems*. Cambridge University Press, 2015. 5

[81] Graham T Reed. *Silicon photonics: the state of the art*. John Wiley & Sons, 2008. 5

[82] Wim Bogaerts, Martin Fiers, and Pieter Dumon. **Design challenges in silicon photonics**. *IEEE Journal of Selected Topics in Quantum Electronics*, **20**(4):1–8, 2014. 5

[83] Zhou Fang and Ce Zhou Zhao. **Recent progress in silicon photonics: a review**. *ISRN Optics*, **2012**, 2012. 5

[84] Philippe P Absil, Peter Verheyen, Peter De Heyn, Marianna Pantouvaki, Guy Lepage, Jeroen De Coster, and Joris Van Campenhout. **Silicon photonics integrated circuits: a manufacturing platform for high density, low power optical I/Os**. *Optics Express*, **23**(7):9369–9378, 2015. 5

[85] Harish Subbaraman, Xiaochuan Xu, Amir Hosseini, Xingyu Zhang, Yang Zhang, David Kwong, and Ray T Chen. **Recent advances in silicon-based passive and active optical interconnects**. *Optics Express*, **23**(3):2487–2511, 2015. 5, 7

[86] T Shoji, T Tsuchizawa, T Watanabe, K Yamada, and H Morita. **Low loss mode size converter from 0.3 μm square Si wire waveguides to singlemode fibres**. *Electronics Letters*, **38**(25):1669–1670, 2002. 6

[87] Vilson R Almeida, Roberto R Panepucci, and Michal Lipson. **Nanotaper for compact mode conversion**. *Optics Letters*, **28**(15):1302–1304, 2003. 6

[88] Long Chen, Christopher R Doerr, Young-Kai Chen, and Tsung-Yang Liow. **Low-Loss and Broadband Cantilever Couplers Between Standard Cleaved Fibers and High-Index-Contrast Si _{3} N _{4} or Si Waveguides**. *IEEE Photonics Technology Letters*, **22**(23):1744–1746, 2010. 6

[89] Qing Fang, Tsung-Yang Liow, Jun Feng Song, Chee Wei Tan, Ming Bin Yu, Guo Qiang Lo, and Dim-Lee Kwong. **Suspended optical fiber-to-waveguide mode size converter for silicon photonics**. *Optics Express*, **18**(8):7763–7769, 2010. 6

[90] Michael Wood, Peng Sun, and Ronald M Reano. **Compact cantilever couplers for low-loss fiber coupling to silicon photonic integrated circuits**. *Optics Express*, **20**(1):164–172, 2012. 6

[91] R Takei, M Suzuki, E Omoda, S Manako, T Kamei, M Mori, and Y Sakakibara. **Silicon knife-edge taper waveguide for ultralow-loss spot-size converter fabricated by photolithography**. *Applied Physics Letters*, **102**(10):101108, 2013. 6

[92] Nobuaki Hatori, Takanori Shimizu, Makoto Okano, Masashige Ishizaka, Tsuyoshi Yamamoto, Yutaka Urino, Masahiko Mori, Takahiro Nakamura, and Yasuhiko Arakawa. **A hybrid integrated light source on a silicon platform using a trident spot-size converter**. *Journal of Lightwave Technology*, **32**(7):1329–1336, 2014. 6

[93] Jing Wang, Yi Xuan, Chunghun Lee, Ben Niu, Lei Liu, Gordon Ning Liu, and Minghao Qi. **Low-loss and misalignment-tolerant fiber-to-chip edge coupler based on double-tip inverse tapers**. In *Optical Fiber Communications Conference*, pages 1–3. IEEE, 2016. 6

[94] Hyundai Park, Sanggi Kim, Jaegyu Park, Jiho Joo, and Gyungock Kim. **A fiber-to-chip coupler based on Si/SiON cascaded tapers for Si photonic chips**. *Optics Express*, **21**(24):29313–29319, 2013. 6

[95] Amnon Yariv and Michiharu Nakamura. **Periodic structures for integrated optics**. *IEEE Journal of Quantum Electronics*, **13**(4):233–253, 1977. 6

[96] Frederik Van Laere, Günther Roelkens, Jonathan Schrauwen, Dirk Taillaert, Pieter Dumon, Wim Bogaerts, Dries Van Thourhout, and Roel Baets. **Compact grating couplers between optical fibers and Silicon-on-Insulator photonic wire waveguides with 69% coupling efficiency**. In *Optical Fiber Communication Conference*, pages 1–3. IEEE, 2006. 6

[97] Bernd Schmid, Alexander Petrov, and Manfred Eich. **Optimized grating coupler with fully etched slots**. *Optics Express*, **17**(13):11066–11076, 2009. 6

[98] Mikael Antelius, Kristinn B Gylfason, and Hans Sohlström. **An apodized SOI waveguide-to-fiber surface grating coupler for single lithography silicon photonics**. *Optics Express*, **19**(4):3592–3598, 2011. 6

[99] Ruizhi Shi, Hang Guan, Ari Novack, Matthew Streshinsky, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg. **High-Efficiency Grating Couplers Near 1310 nm Fabricated by 248-nm DUV Lithography**. *IEEE Photonics Technology Letters*, **15**(26):1569–1572, 2014. 6

[100] Dirk Taillaert, Peter Bienstman, and Roel Baets. **Compact efficient broadband grating coupler for silicon-on-insulator waveguides**. *Optics Letters*, **29**(23):2749–2751, 2004. 6

[101] Günther Roelkens, Dries Van Thourhout, and Roel Baets. **High efficiency Silicon-on-Insulator grating coupler based on a poly-Silicon overlay**. *Optics Express*, **14**(24):11622–11630, 2006. 6, 16

[102] Xiaochuan Xu, Harish Subbaraman, John Covey, David Kwong, Amir Hosseini, and Ray T Chen. **Colorless grating couplers realized by interleaving dispersion engineered subwavelength structures**. *Optics Letters*, **38**(18):3588–3591, 2013. 6

[103] Xia Chen, Ke Xu, Zhenzhou Cheng, Christy KY Fung, and Hon K Tsang. **Wideband subwavelength gratings for coupling between silicon-on-insulator waveguides and optical fibers**. *Optics Letters*, **37**(17):3483–3485, 2012. 6

[104] Qiuhang Zhong, Wei Shi, Yun Wang, Lukas Chrostowski, and David V Plant. **An ultra-broadband fiber grating coupler with focusing curved subwavelength structures**. In *Optical Fiber Communication Conference*, pages Th2A–15. Optical Society of America, 2014. 6

[105] JZ Huang, R Scarmozzino, and RM Osgood. **A new design approach to large input/output number multimode interference couplers and its application to low-crosstalk WDM routers**. *IEEE Photonics Technology Letters*, **10**(9):1292–1294, 1998. 6

[106] Louise F Frellsen, Yunhong Ding, Ole Sigmund, and Lars H Frandsen. **Topology optimized mode multiplexing in silicon-on-insulator photonic wire waveguides**. *Optics Express*, **24**(15):16866–16873, 2016. 6

[107] Maurus Bachmann, Pierre A Besse, and Hans Melchior. **General self-imaging properties in N× N multimode interference couplers including phase relations**. *Applied Optics*, **33**(18):3905–3911, 1994. 6, 30

[108] KK Chung, HP Chan, and PL Chu. **A 1× 4 polarization and wavelength independent optical power splitter based on a novel wide-angle low-loss Y-junction**. *Optics Communications*, **267**(2):367–372, 2006. 6

[109] SH Tao, Q Fang, JF Song, MB Yu, GQ Lo, and DL Kwong. **Cascade wide-angle Y-junction 1× 16 optical power splitter based on silicon wire waveguides on silicon-on-insulator**. *Optics Express*, **16**(26):21456–21461, 2008. 6

[110] PD Trinh, S Yegnanarayanan, and B Jalali. **Integrated optical directional couplers in silicon-on-insulator**. *Electronics Letters*, **31**(24):2097–2098, 1995. 6, 16

[111] Liang Cao, Ali Elshaari, Abdelsalam Aboketaf, and Stefan Preble. **Adiabatic couplers in SOI waveguides**. In *Lasers and Electro-Optics (CLEO) and Quantum Electronics and Laser Science Conference (QELS), 2010 Conference on*, pages 1–2. IEEE, 2010. 6

[112] Michael R Watts, Jie Sun, Christopher DeRose, Douglas C Trotter, Ralph W Young, and Gregory N Nielson. **Adiabatic thermo-optic Mach–Zehnder switch**. *Optics Letters*, **38**(5):733–735, 2013. 6

[113] Kimmo Solehmainen, Markku Kapulainen, Mikko Harjanne, and Timo Aalto. **Adiabatic and multimode interference couplers on silicon-on-insulator**. *IEEE Photonics Technology Letters*, **18**(21):2287–2289, 2006. 6

[114] Jiejiang Xing, Zhiyong Li, Yude Yu, and Jinzhong Yu. **Design of polarization-independent adiabatic splitters fabricated on silicon-on-insulator substrates**. *Optics Express*, **21**(22):26729–26734, 2013. 6

[115] Q Lai, M Bachmann, W Hunziker, PA Besse, and H Melchior. **Arbitrary ratio power splitters using angled silica on silicon multimode interference couplers**. *Electronics Letters*, **32**(17):1576–1577, 1996. 6

[116] David JY Feng, TS Lay, and TY Chang. **Waveguide couplers with new power splitting ratios made possible by cascading of short multimode interference sections**. *Optics Express*, **15**(4):1588–1593, 2007. 6

[117] Qingzhong Deng, Lu Liu, Xinbai Li, and Zhiping Zhou. **Arbitrary-ratio 1× 2 power splitter based on asymmetric multimode interference**. *Optics Letters*, **39**(19):5590–5593, 2014. 6

[118] Wim Bogaerts, Pieter Dumon, Dries Van Thourhout, Dirk Taillaert, Patrick Jaenen, Johan Wouters, Stephan Beckx, Vincent Wiaux, and Roel G Baets. **Compact wavelength-selective functions in silicon-on-insulator photonic wires**. *IEEE Journal of Selected Topics in Quantum Electronics*, **12**(6):1394–1401, 2006. 7

[119] Long Chen, Christopher R Doerr, Po Dong, and Young-kai Chen. **Monolithic silicon chip with 10 modulator channels at 25 Gbps and 100-GHz spacing**. *Optics Express*, **19**(26):B946–B951, 2011. 7

[120] Stanley Cheung, Tiehui Su, Katsunari Okamoto, and SJB Yoo. **Ultra-compact silicon photonic 512× 512 25 GHz arrayed waveguide grating router**. *IEEE Journal of Selected Topics in Quantum Electronics*, **20**(4):310–316, 2014. 7

REFERENCES

[121] Tatsuhiko Fukazawa, Fumiaki Ohno, and Toshihiko Baba. **Very compact arrayed-waveguide-grating demultiplexer using Si photonic wire waveguides**. *Japanese Journal of Applied Physics*, **43**(5B):L673, 2004. 7

[122] Pavel Cheben, JH Schmid, André Delâge, Adam Densmore, Siegfried Janz, Boris Lamontagne, J Lapointe, Edith Post, Philip Waldron, and D-X Xu. **A high-resolution silicon-on-insulator arrayed waveguide grating microspectrometer with sub-micrometer aperture waveguides**. *Optics Express*, **15**(5):2299–2306, 2007. 7

[123] Corrado Sciancalepore, Richard John Lycett, Jacques A Dallery, Sebastien Pauliac, Karim Hassan, Julie Harduin, Hélène Duprez, Ulf Weidenmueller, Dominic FG Gallagher, Sylvie Menezo, et al. **Low-crosstalk fabrication-insensitive echelle grating demultiplexers on silicon-on-insulator**. *IEEE Photonics Technology Letters*, **27**(5):494–497, 2015. 7

[124] Dazeng Feng, Wei Qian, Hong Liang, Cheng-Chih Kung, Joan Fong, B Jonathan Luff, and Mehdi Asghari. **Fabrication insensitive echelle grating in silicon-on-insulator platform**. *IEEE Photonics Technology Letters*, **23**(5):284–286, 2011. 7

[125] Wim Bogaerts, Shankar Kumar Selvaraja, Pieter Dumon, Joost Brouckaert, Katrien De Vos, Dries Van Thourhout, and Roel Baets. **Silicon-on-insulator spectral filters fabricated with CMOS technology**. *IEEE Journal of Selected Topics in Quantum Electronics*, **16**(1):33–44, 2010. 7

[126] Folkert Horst, William MJ Green, Bert Jan Offrein, and Yurii A Vlasov. **Silicon-on-insulator echelle grating WDM demultiplexers with two stigmatic points**. *IEEE Photonics Technology Letters*, **21**(23):1743–1745, 2009. 7

[127] Shijun Xiao, Maroof H Khan, Hao Shen, and Minghao Qi. **A highly compact third-order silicon microring add-drop filter with a very large free spectral range, a flat passband and a low delay dispersion**. *Optics Express*, **15**(22):14765–14771, 2007. 7

[128] Qianfan Xu, Brad Schmidt, Jagat Shakya, and Michal Lipson. **Cascaded silicon micro-ring modulators for WDM optical interconnection**. *Optics Express*, **14**(20):9431–9436, 2006. 7

[129] Andreas Vorckel, Mathias Monster, Wolfgang Henschel, P Haring Bolivar, and Heinrich Kurz. **Asymmetrically coupled silicon-on-insulator microring resonators for compact add-drop multiplexers**. *IEEE Photonics Technology Letters*, **15**(7):921–923, 2003. 7

[130] Shijun Xiao, Maroof H Khan, Hao Shen, and Minghao Qi. **Silicon-on-insulator microring add-drop filters with free spectral ranges over 30 nm**. *Journal of Lightwave Technology*, **26**(2):228–236, 2008. 7

[131] Riyadh Dakhil Mansoor, Hugh Sasse, Mohammed Al Asadi, Stephen J Ison, and Alistair P Duffy. **Over coupled ring resonator-based add/drop filters**. *IEEE Journal of Quantum Electronics*, **50**(8):598–604, 2014. 7

[132] Minming Geng, Lianxi Jia, Lei Zhang, Lin Yang, Ping Chen, and Yuliang Liu. **Compact four-channel reconfigurable optical add-drop multiplexer using silicon photonic wire**. *Optics Communications*, **282**(17):3477–3480, 2009. 7

[133] Trung-Thanh Le and Laurence W Cahill. **The Design of 4×× 4 4 Multimode Interference Coupler Based Microring Resonators on an SOI Platform**. *Journal of Telecommunications and Information Technology*, pages 58–62, 2009. 7

[134] Y Painchaud, M Poulin, C Latrasse, and M-J Picard. **Bragg grating based Fabry-Perot filters for characterizing silicon-on-insulator waveguides**. In *Group IV Photonics (GFP), 2012 IEEE 9th International Conference on*, pages 180–182. IEEE, 2012. 7

[135] Xiaomeng Sun, Linjie Zhou, Jingya Xie, Zhi Zou, Liangjun Lu, Haike Zhu, Xinwan Li, and Jianping Chen. **Tunable silicon Fabry–Perot comb filters formed by Sagnac loop mirrors**. *Optics Letters*, **38**(4):567–569, 2013. 7

[136] M Iodice, G Cocorullo, FG Della Corte, and I Rendina. **Silicon Fabry–Perot filter for WDM systems channels monitoring**. *Optics Communications*, **183**(5-6):415–418, 2000. 7

[137] Marcus S Dahlem, Charles W Holzwarth, Anatol Khilo, Franz X Kärtner, Henry I Smith, and Erich P Ippen. **Reconfigurable multi-channel second-order silicon microring-resonator filterbanks for on-chip WDM systems**. *Optics Express*, **19**(1):306–316, 2011. 7

[138] Wim Bogaerts, Peter De Heyn, Thomas Van Vaerenbergh, Katrien De Vos, Shankar Kumar Selvaraja, Tom Claes, Pieter Dumon, Peter Bienstman, Dries Van Thourhout, and Roel Baets. **Silicon microring resonators**. *Laser & Photonics Reviews*, **6**(1):47–73, 2012. 7, 55

[139] Cheng Li, Rui Bai, Ayman Shafik, Ehsan Zhian Tabasy, Binhao Wang, Geng Tang, Chao Ma, Chin-Hui Chen, Zhen Peng, Marco Fiorentino, et al. **Silicon photonic transceiver circuits with microring resonator bias-based wavelength stabilization in 65 nm CMOS**. *IEEE Journal of Solid-State Circuits*, **49**(6):1419–1436, 2014. 7

[140] Junbo Yang, Zhengzheng Shao, Kuo Zhou, Suzhi Xu, and Jia Xu. **High performance and compact polarization beam splitter based on silicon-on-insulator subwavelength grating coupler**. In *2013 International Conference on Optical Instruments and Technology: Micro/Nano Photonics and Fabrication*, **9047**, page 90470D. International Society for Optics and Photonics, 2013. 7

[141] Yongbo Tang, Daoxin Dai, and Sailing He. **Proposal for a grating waveguide serving as both a polarization splitter and an efficient coupler for silicon-on-insulator nanophotonic circuits**. *IEEE Photonics Technology Letters*, **21**(4):242–244, 2009. 7

[142] Wissem Sfar Zaoui, Andreas Kunze, Wolfgang Vogel, and Manfred Berroth. **CMOS-compatible polarization splitting grating couplers with a backside metal mirror**. *IEEE Photonics Technology Letters*, **25**(14):1395–1397, 2013. 7

[143] Matthew Streshinsky, Ruizhi Shi, Ari Novack, Roger Tern Poh Cher, Andy Eu-Jin Lim, Patrick Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg. **A compact bi-wavelength polarization splitting grating coupler fabricated in a 220 nm SOI platform**. *Optics Express*, **21**(25):31019–31028, 2013. 7

[144] Dirk Taillaert, Harold Chong, Peter I Borel, Lars H Frandsen, Richard M De La Rue, and Roel Baets. **A compact two-dimensional grating coupler used as a polarization splitter**. *IEEE Photonics Technology Letters*, **15**(9):1249–1251, 2003. 7, 17

[145] Yule Xiong, Dan-Xia Xu, Jens H Schmid, Pavel Cheben, Siegfried Janz, and N Ye Winnie. **Fabrication tolerant and broadband polarization splitter and rotator based on a taper-etched directional coupler**. *Optics Express*, **22**(14):17458–17465, 2014. 7

[146] Yawen Huang, Zhao Tu, Huaxiang Yi, Yanping Li, Xingjun Wang, and Weiwei Hu. **High extinction ratio polarization beam splitter with multimode interference coupler on SOI**. *Optics Communications*, **307**:46–49, 2013. 7

[147] Byung-Ki Yang, Sang-Yung Shin, and Daming Zhang. **Ultrashort polarization splitter using two-mode interference in silicon photonic wires**. *IEEE Photonics Technology Letters*, **21**(7):432–434, 2009. 7

[148] Jung Moo Hong, Hyun Ho Ryu, Soon Ryong Park, Jae Wan Jeong, Seung Gol Lee, El-Hang Lee, Se-Geun Park, Deokha Woo, Sunho Kim, and O Beom-Hoan. **Design and fabrication of a significantly shortened multimode interference coupler for polarization splitter application**. *IEEE Photonics Technology Letters*, **15**(1):72–74, 2003. 7

[149] Isa Kiyat, Atilla Aydinli, and Nadir Dagli. **A compact silicon-on-insulator polarization splitter**. *IEEE Photonics Technology Letters*, **17**(1):100–102, 2005. 7

[150] Luc M Augustin, Jos JGM van der Tol, Rabah Hanfoug, Wim JM de Laat, Michael JE van de Moosdijk, Paul WL van Dijk, Yok-Siang Oei, and Meint K Smit. **A single etch-step fabrication-tolerant polarization splitter**. *Journal of Lightwave Technology*, **25**(3):740–746, 2007. 7

[151] Andrei V Tsarev. **Efficient silicon wire waveguide crossing with negligible loss and crosstalk**. *Optics Express*, **19**(15):13732–13737, 2011. 7

[152] Adam M Jones, Christopher T DeRose, Anthony L Lentine, Douglas C Trotter, Andrew L Starbuck, and Robert A Norwood. **Ultra-low crosstalk, CMOS compatible waveguide crossings for densely integrated photonic interconnection networks**. *Optics Express*, **21**(10):12002–12013, 2013. 7

[153] Przemek J Bock, Pavel Cheben, Jens H Schmid, Jean Lapointe, André Delâge, Dan-Xia Xu, Siegfried Janz, Adam Densmore, and Trevor J Hall. **Subwavelength grating crossings for silicon wire waveguides**. *Optics Express*, **18**(15):16146–16155, 2010. 7, 8

[154] Hui Chen and Andrew W Poon. **Low-loss multimode-interference-based crossings for silicon wire waveguides**. *IEEE Photonics Technology Letters*, **18**(21):2260–2262, 2006. 7

[155] Heliang Liu, Hwayaw Tam, PKA Wai, and Edwin Pun. **Low-loss waveguide crossing using a multimode interference structure**. *Optics Communications*, **241**(1-3):99–104, 2004. 7

[156] Chyong-Hua Chen and Chia-Hsiang Chiu. **Taper-integrated multimode-interference based waveguide crossing design**. *IEEE Journal of Quantum Electronics*, **46**(11):1656–1661, 2010. 7

[157] Sang-Hun Kim, Guangwei Cong, Hitoshi Kawashima, Toshifumi Hasama, and Hiroshi Ishikawa. **Tilted MMI crossings based on silicon wire waveguide**. *Optics Express*, **22**(3):2545–2552, 2014. 7

[158] Milos A Popovic, Erich P Ippen, and Franz X Kartner. **Low-loss Bloch waves in open structures and highly compact, efficient Si waveguide-crossing arrays**. In *Lasers and Electro-Optics Society, 2007. LEOS 2007. The 20th Annual Meeting of the IEEE*, pages 56–57. IEEE, 2007. 7

[159] Yang Zhang, Amir Hosseini, Xiaochuan Xu, David Kwong, and Ray T Chen. **Ultralow-loss silicon waveguide crossing using Bloch modes in index-engineered cascaded multimode-interference couplers**. *Optics Letters*, **38**(18):3608–3611, 2013. 7

[160] Yangjin Ma, Yi Zhang, Shuyu Yang, Ari Novack, Ran Ding, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg. **Ultralow loss single layer submicron silicon waveguide crossing for SOI optical interconnect**. *Optics Express*, **21**(24):29374–29382, 2013. 7, 16, 19, 34

[161] Pablo Sanchis, Pablo Villalba, Francisco Cuesta, Andreas Håkansson, Amadeu Griol, José V Galán, Antoine Brimont, and Javier Martí. **Highly efficient crossing structure for silicon-on-insulator waveguides**. *Optics Letters*, **34**(18):2760–2762, 2009. 7, 16

[162] Philippe Lalanne and Jean-Paul Hugonin. **High-order effective-medium theory of subwavelength gratings in classical mounting: application to volume holograms**. *JOSA A*, **15**(7):1843–1851, 1998. 8

[163] Robert Halir, Przemek J Bock, Pavel Cheben, Alejandro Ortega-Moñux, Carlos Alonso-Ramos, Jens H Schmid, Jean Lapointe, Dan-Xia Xu, J Gonzalo Wangüemert-Pérez, Íñigo Molina-Fernández, et al. **Waveguide subwavelength structures: a review of principles and applications**. *Laser & Photonics Reviews*, **9**(1):25–49, 2015. 8

[164] Graham T Reed, G Mashanovich, FY Gardes, and DJ Thomson. **Silicon optical modulators**. *Nature Photonics*, **4**(8):518, 2010. 8

[165] Jeremy Witzens. **Silicon photonics: Modulators make efficiency leap**. *Nature Photonics*, **11**(8):459, 2017. 8

[166] David J Thomson, Frederic Y Gardes, Jean-Marc Fedeli, Sanja Zlatanovic, Youfang Hu, Bill Ping Piu Kuo, Evgeny Myslivets, Nikola Alic, Stojan Radic, Goran Z Mashanovich, et al. **50-Gb/s silicon optical modulator**. *IEEE Photonics Technology Letters*, **24**(4):234–236, 2012. 8

REFERENCES

[167] Graham T Reed, Goran Z Mashanovich, Frederic Y Gardes, Milos Nedeljkovic, Youfang Hu, David J Thomson, Ke Li, Peter R Wilson, Sheng-Wen Chen, and Shawn S Hsu. **Recent breakthroughs in carrier depletion based silicon optical modulators**. *Nanophotonics*, **3**(4-5):229–245, 2014. 8

[168] RICHARDA Soref and BRIANR Bennett. **Electrooptical effects in silicon**. *IEEE Journal of Quantum Electronics*, **23**(1):123–129, 1987. 8

[169] Po Dong, Long Chen, and Young-kai Chen. **High-speed low-voltage single-drive push-pull silicon Mach-Zehnder modulators**. *Optics Express*, **20**(6):6163–6169, 2012. 8

[170] Xi Xiao, Hao Xu, Xianyao Li, Zhiyong Li, Tao Chu, Yude Yu, and Jinzhong Yu. **High-speed, low-loss silicon Mach–Zehnder modulators with doping optimization**. *Optics Express*, **21**(4):4116–4125, 2013. 8

[171] M Webster, P Gothoskar, V Patel, D Piede, S Anderson, R Tummidi, D Adams, C Appel, P Metz, S Sunder, et al. **An efficient MOS-capacitor based silicon modulator and CMOS drivers for optical transmitters**. In *Group IV Photonics (GFP), 2014 IEEE 11th International Conference on*, pages 1–2. IEEE, 2014. 8

[172] Mark A Webster, Kumar Lakshmikumar, Craig Appel, Bipin Dama, Kal Shastri, et al. **Low-power MOS-capacitor based silicon photonic modulators and CMOS drivers**. In *Optical Fiber Communication Conference*, pages W4H–3. Optical Society of America, 2015. 8

[173] Biljana Milivojevic, Stefan Wiese, James Whiteaway, Christian Raabe, Anujit Shastri, Mark Webster, Peter Metz, Sanjay Sunder, Bill Chattin, Sean P Anderson, et al. **Silicon high speed modulator for advanced modulation: device structures and exemplary modulator performance**. In *Silicon Photonics IX*, **8990**, page 899013. International Society for Optics and Photonics, 2014. 8

[174] Brian R Bennett, Richard A Soref, and Jesus A Del Alamo. **Carrier-induced change in refractive index of InP, GaAs and InGaAsP**. *IEEE Journal of Quantum Electronics*, **26**(1):113–122, 1990. 8

[175] Laurent Chusseau, Patrick Martin, Céline Brasseur, Claude Alibert, Philippe Hervé, Philippe Arguel, Françoise Lozes-Dupuy, and EVK Rao. **Carrier-induced change due to doping in refractive index of InP: Measurements at 1.3 and 1.5 μm**. *Applied Physics Letters*, **69**(20):3054–3056, 1996. 8

[176] D Botteldooren and R Baets. **Influence of band-gap shrinkage on the carrier-induced refractive index change in InGaAsP**. *Applied Physics Letters*, **54**(20):1989–1991, 1989. 8

[177] C Hilsum. **Simple empirical relationship between mobility and carrier concentration**. *Electronics Letters*, **10**(13):259–260, 1974. 8

[178] Tatsurou Hiraki, Takuma Aihara, Koichi Hasebe, Koji Takeda, Takuro Fujii, Takaaki Kakitsuka, Tai Tsuchizawa, Hiroshi Fukuda, and Shinji Matsuo. **Heterogeneously integrated iii–v/Si MOS capacitor Mach–Zehnder modulator**. *Nature Photonics*, **11**(8):482, 2017. 8

[179] Jae-Hoon Han, Frederic Boeuf, Junichi Fujikata, Shigeki Takahashi, Shinichi Takagi, and Mitsuru Takenaka. **Efficient low-loss InGaAsP/Si hybrid MOS optical modulator**. *Nature Photonics*, **11**(8):486, 2017. 8

[180] Shashank Gupta, Srinivasan Ashwyn Srinivasan, Marianna Pantouvaki, Hongtao Chen, Peter Verheyen, Guy Lepage, Dries V Thourhout, Gunther Roelkens, Krishna Saraswat, Philippe Absil, et al. **50GHz Ge waveguide electro-absorption modulator integrated in a 220nm SOI photonics platform**. In *Optical Fiber Communication Conference*, pages Tu2A–4. Optical Society of America, 2015. 8

[181] Papichaya Chaisakul, Delphine Marris-Morini, Mohamed-Said Rouifed, Jacopo Frigerio, Daniel Chrastina, Jean-René Coudevylle, Xavier Le Roux, Samson Edmond, Giovanni Isella, and Laurent Vivien. **Recent progress in GeSi electro-absorption modulators**. *Science and Technology of Advanced Materials*, **15**(1):014601, 2013. 8

[182] Lorenzo Mastronardi, Mehdi Banakar, AZ Khokhar, Nannicha Hattasan, Teerapat Rutirawut, T Domínguez Bucio, KM Grabska, Callum Littlejohns, Alexandre Bazin, Goran Mashanovich, et al. **High-speed Si/GeSi hetero-structure Electro Absorption Modulator**. *Optics Express*, **26**(6):6663–6673, 2018. 8

[183] Baohu Huang, Weibing Lu, Zhenguo Liu, and Siping Gao. **Low-energy high-speed plasmonic enhanced modulator using graphene**. *Optics Express*, **26**(6):7358–7367, 2018. 9

[184] Tao Yin, Rami Cohen, Mike M Morse, Gadi Sarid, Yoel Chetrit, Doron Rubin, and Mario J Paniccia. **31GHz Ge nip waveguide photodetectors on Silicon-on-Insulator substrate**. *Optics Express*, **15**(21):13965–13971, 2007. 9

[185] Laurent Vivien, Johann Osmond, Jean-Marc Fédéli, Delphine Marris-Morini, Paul Crozat, Jean-François Damlencourt, Eric Cassan, Y Lecunff, and Suzanne Laval. **42 GHz pin Germanium photodetector integrated in a silicon-on-insulator waveguide**. *Optics Express*, **17**(8):6252–6257, 2009. 9

[186] Solomon Assefa, Fengnian Xia, Stephen W Bedell, Ying Zhang, Teya Topuria, Philip M Rice, and Yurii A Vlasov. **CMOS-integrated high-speed MSM germanium waveguide photodetector**. *Optics Express*, **18**(5):4986–4999, 2010. 9

[187] Shirong Liao, Ning-Ning Feng, Dazeng Feng, Po Dong, Roshanak Shafiiha, Cheng-Chih Kung, Hong Liang, Wei Qian, Yong Liu, Joan Fong, et al. **36 GHz submicron silicon waveguide germanium photodetector**. *Optics Express*, **19**(11):10967–10972, 2011. 9

[188] Christopher T DeRose, Douglas C Trotter, William A Zortman, Andrew L Starbuck, Moz Fisher, Michael R Watts, and Paul S Davids. **Ultra compact 45 GHz CMOS compatible Germanium waveguide photodiode with low dark current**. *Optics Express*, **19**(25):24897–24904, 2011. 9

[189] Guoliang Li, Ying Luo, Xuezhe Zheng, Gianlorenzo Masini, Attila Mekis, Subal Sahni, Hiren Thacker, Jin Yao, Ivan Shubin, Kannan Raj, et al. **Improving CMOS-compatible Germanium photodetectors**. *Optics Express*, **20**(24):26345–26350, 2012. 9

[190] Léopold Virot, Daniel Benedikovic, Bertrand Szelag, Carlos Alonso-Ramos, Bayram Karakus, Jean-Michel Hartmann, Xavier Le Roux, Paul Crozat, Eric Cassan, Delphine Marris-Morini, et al. **Integrated waveguide PIN photodiodes exploiting lateral Si/Ge/Si heterojunction**. *Optics Express*, **25**(16):19487–19496, 2017. 9

[191] Hongtao Chen, P Verheyen, Peter De Heyn, G Lepage, J De Coster, S Balakrishnan, P Absil, W Yao, L Shen, Günther Roelkens, et al. **- 1 V bias 67 GHz bandwidth Si-contacted germanium waveguide pin photodetector for optical links at 56 Gbps and beyond**. *Optics Express*, **24**(5):4622–4631, 2016. 9

[192] Ryan Going, Tae Joon Seok, Jodi Loo, Kyle Hsu, and Ming C Wu. **Germanium wrap-around photodetectors on Silicon photonics**. *Optics Express*, **23**(9):11975–11984, 2015. 9

[193] Yi Zhang, Shuyu Yang, Yisu Yang, Michael Gould, Noam Ophir, Andy Eu-Jin Lim, Guo-Qiang Lo, Peter Magill, Keren Bergman, Tom Baehr-Jones, et al. **A high-responsivity photodetector absent metal-germanium direct contact**. *Optics Express*, **22**(9):11367–11375, 2014. 9

[194] Tsung-Yang Liow, Ning Duan, Andy Eu-Jin Lim, Xiaoguang Tu, Mingbin Yu, and Guo-Qiang Lo. **Waveguide Ge/Si avalanche photodetector with a unique low-height-profile device structure**. In *Optical Fiber Communications Conference and Exhibition (OFC), 2014*, pages 1–3. IEEE, 2014. 9

[195] Hong Tao Chen, Peter Verheyen, Peter De Heyn, Guy Lepage, Jeroen De Coster, Philippe Absil, Gunther Roelkens, and Joris Van Campenhout. **High-responsivity low-voltage 28-Gb/s Ge pin photodetector with silicon contacts**. *Journal of Lightwave Technology*, **33**(4):820–824, 2015. 9

[196] Stefan Lischke, Dieter Knoll, Christian Mai, Lars Zimmermann, Anna Peczek, Marcel Kroh, Andreas Trusch, Edgar Krune, Karsten Voigt, and A Mai. **High bandwidth, high responsivity waveguide-coupled germanium pin photodiode**. *Optics Express*, **23**(21):27213–27220, 2015. 9

[197] Matthew J Byrd, Erman Timurdogan, Zhan Su, Christopher V Poulton, Nicholas M Fahrenkopf, Gerald Leake, Douglas D Coolbaugh, and Michael R Watts. **Mode-evolution-based coupler for high saturation power Ge-on-Si photodetectors**. *Optics Letters*, **42**(4):851–854, 2017. 9

[198] Po Dong, Shirong Liao, Hong Liang, Roshanak Shafiiha, Dazeng Feng, Guoliang Li, Xuezhe Zheng, Ashok V Krishnamoorthy, and Mehdi Asghari. **Submilliwatt, ultrafast and broadband electro-optic silicon switches**. *Optics Express*, **18**(24):25225–25231, 2010. 9

[199] Min Yang, William MJ Green, Solomon Assefa, Joris Van Campenhout, Benjamin G Lee, Christopher V Jahnes, Fuad E Doany, Clint L Schow, Jeffrey A Kash, and Yurii A Vlasov. **Non-blocking 4x4 electro-optic silicon switch for on-chip photonic networks**. *Optics Express*, **19**(1):47–54, 2011. 9

[200] Joris Van Campenhout, William MJ Green, Solomon Assefa, and Yurii A Vlasov. **Low-power, 2× 2 silicon electro-optic switch with 110-nm bandwidth for broadband reconfigurable optical networks**. *Optics Express*, **17**(26):24020–24029, 2009. 9

[201] Keijiro Suzuki, Guangwei Cong, Ken Tanizawa, Sang-Hun Kim, Shu Namiki, and Hitoshi Kawashima. **50-dB extinction-ratio in 2× 2 silicon optical switch with variable splitter**. In *Lasers and Electro-Optics (CLEO), 2014 Conference on*, pages 1–2. IEEE, 2014. 9

[202] Yurii Vlasov, William MJ Green, and Fengnian Xia. **High-throughput silicon nanophotonic wavelength-insensitive switch for on-chip optical networks**. *Nature Photonics*, **2**(4):242, 2008. 9, 71

[203] Xuan Wang, Jose A Martinez, Magdalena S Nawrocka, and Roberto R Panepucci. **Compact thermally tunable silicon wavelength switch: modeling and characterization**. *IEEE Photonics Technology Letters*, **20**(11):936–938, 2008. 9

[204] William S Fegadolli, German Vargas, Xuan Wang, Felipe Valini, Luis AM Barea, José EB Oliveira, Newton Frateschi, Axel Scherer, Vilson R Almeida, and Roberto R Panepucci. **Reconfigurable silicon thermo-optical ring resonator switch based on Vernier effect control**. *Optics Express*, **20**(13):14722–14733, 2012. 9

[205] Bing J Sheu, Donald L Scharfetter, P-K Ko, and M-C Jeng. **BSIM: Berkeley short-channel IGFET model for MOS transistors**. *IEEE Journal of Solid-State Circuits*, **22**(4):558–566, 1987. 10

[206] Peter De Dobbelaere, Ali Ayazi, Yuemeng Chi, Anders Dahl, Scott Denton, Steffen Gloeckner, Kam-Yan Hon, Steve Hovey, Yi Liang, Michael Mack, et al. **Packaging of silicon photonics systems**. In *Optical Fiber Communications Conference*, pages 1–3. IEEE, 2014. 11

[207] Bradley Snyder and Peter O'Brien. **Packaging process for grating-coupled silicon photonic waveguides using angle-polished fibers**. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **3**(6):954–959, 2013. 11

[208] Guang-Hua Duan, Christophe Jany, Alban Le Liepvre, Alain Accard, Marco Lamponi, Dalila Make, Peter Kaspar, Guillaume Levaufre, Nils Girard, Francois Lelarge, et al. **Hybrid III–V on Silicon Lasers for Photonic Integrated Circuits on Silicon**. *IEEE Journal of Selected Topics in Quantum Electronics*, **20**(4):158–170, 2014. 11, 52

[209] Elton Marchena, Timothy Creazzo, Stephen B Krasulick, Paul Yu, Derek Van Orden, John Y Spann, Christopher C Blivin, John M Dallesasse, Petros Varangis, Robert J Stone, et al. **Integrated tunable CMOS laser for Si photonics**. In *Optical Fiber Communication Conference*, pages PDP5C–7. Optical Society of America, 2013. 11

[210] Shahram Keyvaninia, Steven Verstuyft, Liesbet Van Landschoot, F Lelarge, G-H Duan, S Messaoudene, JM Fedeli, T De Vries, B Smalbrugge, EJ Geluk, et al. **Heterogeneously integrated III-V/silicon distributed feedback lasers**. *Optics Letters*, **38**(24):5434–5437, 2013. 12

REFERENCES

[211] Alan Y Liu, Robert W Herrick, Osamu Ueda, Pierre M Petroff, Arthur C Gossard, and John E Bowers. **Reliability of InAs/GaAs quantum dot lasers epitaxially grown on silicon**. *IEEE Journal of Selected Topics in Quantum Electronics*, **21**(6):690–697, 2015. 12

[212] Christos Theodoros Santis, Scott T Steger, Yaakov Vilenchik, Arseny Vasilyev, and Amnon Yariv. **High-coherence semiconductor lasers based on integral high-Q resonators in hybrid Si/III-V platforms**. *Proceedings of the National Academy of Sciences*, **111**(8):2879–2884, 2014. 12

[213] Tin Komljenovic, Sudharsanan Srinivasan, Erik Norberg, Michael Davenport, Gregory Fish, and John E Bowers. **Widely tunable narrow-linewidth monolithically integrated external-cavity semiconductor lasers**. *IEEE Journal of Selected Topics in Quantum Electronics*, **21**(6):214–222, 2015. 12

[214] Lucas B Soldano and Erik CM Pennings. **Optical multi-mode interference devices based on self-imaging: principles and applications**. *Journal of Lightwave Technology*, **13**(4):615–627, 1995. 16, 30

[215] Dirk Taillaert, Frederik Van Laere, Melanie Ayre, Wim Bogaerts, Dries Van Thourhout, Peter Bienstman, and Roel Baets. **Grating couplers for coupling between optical fibers and nanophotonic waveguides**. *Japanese Journal of Applied Physics*, **45**(8R):6071, 2006. 16

[216] Thomas Edward Murphy, Jeffrey Todd Hastings, and Henry I Smith. **Fabrication and characterization of narrow-band Bragg-reflection filters in silicon-on-insulator ridge waveguides**. *Journal of Lightwave Technology*, **19**(12):1938, 2001. 16

[217] Graham T Reed and Andrew P Knights. *Silicon photonics: an introduction*. John Wiley & Sons, 2004. 16

[218] Po-Han Fu, Yi-Chou Tu, and Ding-Wei Huang. **Broadband optical waveguide couplers with arbitrary coupling ratios designed using a genetic algorithm**. *Optics Express*, **24**(26):30547–30561, 2016. 16, 89

[219] Yi Zhang, Shuyu Yang, Andy Eu-Jin Lim, Guo-Qiang Lo, Christophe Galland, Tom Baehr-Jones, and Michael Hochberg. **A compact and low loss Y-junction for submicron silicon waveguide**. *Optics Express*, **21**(1):1310–1316, 2013. 16, 19, 34

[220] Hang Guan, Yangjin Ma, Ruizhi Shi, Xiaoliang Zhu, Rick Younce, Yaojia Chen, Jose Roman, Noam Ophir, Yang Liu, Ran Ding, et al. **Compact and low loss 90 degree optical hybrid on a silicon-on-insulator platform**. *Optics Express*, **25**(23):28957–28968, 2017. 16

[221] Chenying Yang, Liang Hong, Weidong Shen, Yueguang Zhang, Xu Liu, and Hongyu Zhen. **Design of reflective color filters with high angular tolerance by particle swarm optimization method**. *Optics Express*, **21**(8):9315–9323, 2013. 16

[222] Jesse Lu and Jelena Vučković. **Nanophotonic computational design**. *Optics Express*, **21**(11):13351–13367, 2013. 17

[223] Alexander Y Piggott, Jesse Lu, Konstantinos G Lagoudakis, Jan Petykiewicz, Thomas M Babinec, and Jelena Vučković. **Inverse design and demonstration of a compact and broadband on-chip wavelength demultiplexer**. *Nature Photonics*, **9**(6):374–377, 2015. 17

[224] Alexander Y Piggott, Jesse Lu, Thomas M Babinec, Konstantinos G Lagoudakis, Jan Petykiewicz, and Jelena Vučković. **Inverse design and implementation of a wavelength demultiplexing grating coupler**. *Scientific Reports*, **4**:7210, 2014. 17, 89

[225] Luluzi Lu, Minming Zhang, Feiya Zhou, Weijie Chang, Jiang Tang, Dongyu Li, Xinshu Ren, Zepeng Pan, Mengfan Cheng, and Deming Liu. **Inverse-designed ultra-compact star-crossings based on PhC-like sub-wavelength structures for optical intercross connect**. *Optics Express*, **25**(15):18355–18364, 2017. 17, 89

[226] Apratim Majumder, Bing Shen, Randy Polson, and Rajesh Menon. **Ultra-compact polarization rotation in integrated silicon photonics using digital metamaterials**. *Optics Express*, **25**(17):19721–19731, 2017. 17, 27, 89

[227] Andreas Hakansson, José Sánchez-Dehesa, and Lorenzo Sanchis. **Inverse design of photonic crystal devices**. *IEEE Journal on Selected Areas in Communications*, **23**(7):1365–1371, 2005. 17

[228] Bing Shen, Peng Wang, Randy Polson, and Rajesh Menon. **An integrated-nanophotonics polarization beamsplitter with 2.4× 2.4 μm 2 footprint**. *Nature Photonics*, **9**(6):378, 2015. 17

[229] Tymon Barwicz, Michael R Watts, Miloš A Popović, Peter T Rakich, Luciano Socci, Franz X Kärtner, Erich P Ippen, and Henry I Smith. **Polarization-transparent microphotonic devices in the strong confinement limit**. *Nature Photonics*, **1**(1):57–60, 2007. 17, 46

[230] Po Dong, Chongjin Xie, Long Chen, Lawrence L Buhl, and Young-Kai Chen. **112-Gb/s monolithic PDM-QPSK modulator in silicon**. *Optics Express*, **20**(26):B624–B629, 2012. 17

[231] Xinying Li, Ze Dong, Jianjun Yu, Jianguo Yu, and Nan Chi. **Heterodyne coherent detection of WDM PDM-QPSK signals with spectral efficiency of 4b/s/Hz**. *Optics Express*, **21**(7):8808–8814, 2013. 17

[232] Wim Bogaerts, Dirk Taillaert, Pieter Dumon, Dries Van Thourhout, Roel Baets, and Elroy Pluk. **A polarization-diversity wavelength duplexer circuit in silicon-on-insulator photonic wires**. *Optics Express*, **15**(4):1567–1578, 2007. 17

[233] Frederik Van Laere, Wim Bogaerts, Pieter Dumon, Günther Roelkens, Dries Van Thourhout, and Roel Baets. **Focusing polarization diversity grating couplers in silicon-on-insulator**. *Journal of Lightwave Technology*, **27**(5):612–618, 2009. 17

[234] Ari Novack, Yang Liu, Ran Ding, Michael Gould, Tom Baehr-Jones, Qi Li, Yisu Yang, Yangjin Ma, Yi Zhang, Kishore Padmaraju, et al. **A 30 GHz silicon photonic platform**. In *Group IV Photonics (GFP), 2013 IEEE 10th International Conference on*, pages 7–8. IEEE, 2013. 17, 37, 47

[235] Mariam Aamer, Ana M Gutierrez, Antoine Brimont, Diedrik Vermeulen, Gunther Roelkens, Jean-Marc Fedeli, Andreas Hakansson, and Pablo Sanchis. **CMOS compatible silicon-on-insulator polarization rotator based on symmetry breaking of the waveguide cross section**. *IEEE Photonics Technology Letters*, **24**(22):2031–2034, 2012. 17

[236] Long Chen, Christopher R Doerr, and Young-Kai Chen. **Compact polarization rotator on silicon for polarization-diversified circuits**. *Optics Letters*, **36**(4):469–471, 2011. 17, 27, 46

[237] Wesley D Sacher, Tymon Barwicz, Benjamin JF Taylor, and Joyce KS Poon. **Polarization rotator-splitters in standard active silicon photonics platforms**. *Optics Express*, **22**(4):3777–3786, 2014. 17, 19, 27

[238] Hang Guan, Ari Novack, Matthew Streshinsky, Ruizhi Shi, Yang Liu, Qing Fang, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg. **High-efficiency low-crosstalk 1310-nm polarization splitter and rotator**. *IEEE Photonics Technology Letters*, **26**(9):925–928, 2014. 17, 19, 20, 46

[239] Hang Guan, Ari Novack, Matthew Streshinsky, Ruizhi Shi, Qing Fang, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg. **CMOS-compatible highly efficient polarization splitter and rotator based on a double-etched directional coupler**. *Optics Express*, **22**(3):2489–2496, 2014. 17

[240] Jing Wang, Ben Niu, Zhen Sheng, Aimin Wu, Xi Wang, Shichang Zou, Minghao Qi, and Fuwan Gan. **Design of a SiO 2 top-cladding and compact polarization splitter-rotator based on a rib directional coupler**. *Optics Express*, **22**(4):4137–4143, 2014. 17

[241] L Sánchez and P Sanchis. **Broadband 8 μm long hybrid silicon-plasmonic transverse magnetic–transverse electric converter with losses below 2 dB**. *Optics Letters*, **38**(15):2842–2845, 2013. 17

[242] Lin Jin, Qin Chen, and Long Wen. **Mode-coupling polarization rotator based on plasmonic waveguide**. *Optics Letters*, **39**(9):2798–2801, 2014. 17

[243] Daoxin Dai and John E Bowers. **Novel concept for ultracompact polarization splitter-rotator based on silicon nanowires**. *Optics Express*, **19**(11):10940–10949, 2011. 19

[244] Daoxin Dai, Yongbo Tang, and John E Bowers. **Mode conversion in tapered submicron silicon ridge optical waveguides**. *Optics Express*, **20**(12):13425–13439, 2012. 19

[245] Daoxin Dai, Jian Wang, and Yaocheng Shi. **Silicon mode (de) multiplexer enabling high capacity photonic networks-on-chip with a single-wavelength-carrier light**. *Optics Letters*, **38**(9):1422–1424, 2013. 19

[246] Yunhong Ding, Jing Xu, Francesco Da Ros, Bo Huang, Haiyan Ou, and Christophe Peucheret. **On-chip two-mode division multiplexing using tapered directional coupler-based mode multiplexer and demultiplexer**. *Optics Express*, **21**(8):10376–10382, 2013. 19

[247] Yunhong Ding, Haiyan Ou, and Christophe Peucheret. **Wideband polarization splitter and rotator with large fabrication tolerance and simple fabrication process**. *Optics Letters*, **38**(8):1227–1229, 2013. 20

[248] Lian-Wee Luo, Noam Ophir, Christine P Chen, Lucas H Gabrielli, Carl B Poitras, Keren Bergmen, and Michal Lipson. **WDM-compatible mode-division multiplexing on a silicon chip**. *Nature Communications*, **5**:3069, 2014. 20

[249] Yingyan Huang, Guoyang Xu, and Seng-Tiong Ho. **An ultracompact optical mode order converter**. *IEEE Photonics Technology Letters*, **18**(21):2281–2283, 2006. 20

[250] Bradley J Frey, Douglas B Leviton, and Timothy J Madison. **Temperature-dependent refractive index of silicon and germanium**. In *Optomechanical Technologies for Astronomy*, **6273**, page 62732J. International Society for Optics and Photonics, 2006. 24

[251] Pieter Dumon. **Ultra-compact integrated optical filters in silicon-on-insulator by means of wafer-scale technology**. *University Gent*, 2007. 24

[252] J Niklas Caspers, J Stewart Aitchison, and Mo Mojahedi. **Experimental demonstration of an integrated hybrid plasmonic polarization rotator**. *Optics Letters*, **38**(20):4054–4057, 2013. 27

[253] Anbang Xie, Linjie Zhou, Jianping Chen, and Xinwan Li. **Efficient silicon polarization rotator based on mode-hybridization in a double-stair waveguide**. *Optics Express*, **23**(4):3960–3970, 2015. 27

[254] Masataka Nakazawa, Kazuro Kikuchi, and Tetsuya Miyazaki. *High spectral density optical communication technologies*, **6**. Springer Science & Business Media, 2010. 30

[255] Kazuro Kikuchi. **Fundamentals of coherent optical fiber communications**. *Journal of Lightwave Technology*, **34**(1):157–179, 2016. 30

[256] Cedric F Lam, Hong Liu, Bikash Koley, Xiaoxue Zhao, Valey Kamalov, and Vijay Gill. **Fiber optic communication technologies: What's needed for datacenter network operations**. *IEEE Communications Magazine*, **48**(7), 2010. 30

[257] Harald Rohde, Erich Gottwald, Antonio Teixeira, Jacklyn Dias Reis, Ali Shahpari, Klaus Pulverer, and Jun Shan Wey. **Coherent ultra dense WDM technology for next generation optical metro and access networks**. *Journal of Lightwave Technology*, **32**(10):2041–2052, 2014. 30

[258] Erik Agrell, Magnus Karlsson, AR Chraplyvy, David J Richardson, Peter M Krummrich, Peter Winzer, Kim Roberts, Johannes Karl Fischer, Seb J Savory, Benjamin J Eggleton, et al. **Roadmap of optical communications**. *Journal of Optics*, **18**(6):063002, 2016. 30

[259] Kimchau N Nguyen, Phillip J Skahan, John M Garcia, Erica Lively, Henrik N Poulsen, Douglas M Baney, and Daniel J Blumenthal. **Monolithically integrated dual-quadrature receiver on InP with 30 nm tunable local oscillator**. *Optics Express*, **19**(26):B716–B721, 2011. 30

REFERENCES

[260] Y Sakamaki, H Yamazaki, T Mizuno, T Goh, Y Nasu, T Hashimoto, S Kamei, K Hattori, and H Takahashi. **One-chip integrated dual polarization optical hybrid using silica-based planar lightwave circuit technology**. In *Optical Communication, 2009. ECOC'09. 35th European Conference on*, pages 1–2. IEEE, 2009. 30

[261] F Gambini, G Meloni, S Faralli, G Contestabile, L Potì, and J Klamkin. **Ultra-compact 56-Gb/s QPSK and 80-Gb/s 16-QAM silicon coherent receiver free of waveguide crossings**. In *Group IV Photonics (GFP), 2014 IEEE 11th International Conference on*, pages 149–150. IEEE, 2014. 30

[262] S Faralli, G Meloni, F Gambini, J Klamkin, L Potì, and G Contestabile. **A compact silicon coherent receiver without waveguide crossing**. *IEEE Photonics Journal*, **7**(4):1–6, 2015. 30

[263] Karsten Voigt, Lars Zimmermann, Georg Winzer, Hui Tian, Bernd Tillack, and Klaus Petermann. ***C*-Band Optical 90° Hybrids in Silicon Nanowaveguide Technology**. *IEEE Photonics Technology Letters*, **23**(23):1769–1771, 2011. 30, 42

[264] Patrick Runge, Stefan Schubert, Angela Seeger, Klemens Janiak, Jens Stephan, Dirk Trommer, Patrick Domburg, and Mads Lønstrup Nielsen. **Monolithic InP receiver chip with a 90° hybrid and 56 GHz balanced photodiodes**. *Optics Express*, **20**(26):B250–B255, 2012. 30

[265] Seok-Hwan Jeong and Ken Morito. **Novel Optical 90° Hybrid Consisting of a Paired Interference Based 2×4 MMI Coupler, a Phase Shifter and a 2×2 MMI Coupler**. *Journal of Lightwave Technology*, **28**(9):1323–1331, 2010. 30, 37, 42

[266] Wei Yang, Mei Yin, Yanping Li, Xingjun Wang, and Ziyu Wang. **Ultra-compact optical 90° hybrid based on a wedge-shaped 2×4 MMI coupler and a 2× 2 MMI coupler in silicon-on-insulator**. *Optics Express*, **21**(23):28423–28431, 2013. 30, 37, 42

[267] Hideki Yagi, Naoko Inoue, Ryuji Masuyama, Takehiko Kikuchi, Tomokazu Katsuyama, Yoshihiro Tateiwa, Katsumi Uesaka, Yoshihiro Yoneda, Masaru Takechi, and Hajime Shoji. **InP-Based pin-Photodiode Array Integrated With 90° Hybrid Using Butt-Joint Regrowth for Compact 100 Gb/s Coherent Receiver**. *IEEE Journal of Selected Topics in Quantum Electronics*, **20**(6):374–380, 2014. 30

[268] Yohei Sakamaki, Takeshi Kawai, Tetsuro Komukai, Mitsunori Fukutoku, Tomoyoshi Kataoka, Toshio Watanabe, and Yuzo Ishii. **Experimental demonstration of multi-degree colorless, directionless, contentionless ROADM for 127-Gbit/s PDM-QPSK transmission system**. *Optics Express*, **19**(26):B1–B11, 2011. 30

[269] D Hoffman, Helmut Heidrich, Gerhard Wenke, R Langenhorst, and Erik Dietrich. **Integrated optics eight-port 90 degrees hybrid on LiNbO/sub 3**. *Journal of Lightwave Technology*, **7**(5):794–798, 1989. 30

[270] Matthias Seimetz and C-M Weinert. **Options, feasibility, and availability of 2/spl times/4 90/spl deg/hybrids for coherent optical systems**. *Journal of Lightwave Technology*, **24**(3):1317–1322, 2006. 30

[271] Seok-Hwan Jeong and Ken Morito. **Simple analytical calculation and experimental demonstration of optical 90° hybrids based on tapered 2× 4 and 2× 2 multimode interference couplers**. *JOSA B*, **28**(1):159–164, 2011. 30, 42

[272] Robert Halir, Günther Roelkens, A Ortega-Moñux, and JG Wangüemert-Pérez. **High-performance 90 hybrid based on a silicon-on-insulator multimode interference coupler**. *Optics Letters*, **36**(2):178–180, 2011. 30, 31, 42

[273] Mohammad R Paiam and Robert I MacDonald. **Design of phased-array wavelength division multiplexers using multimode interference couplers**. *Applied Optics*, **36**(21):5097–5108, 1997. 30

[274] R Adar, CH Henry, MA Milbrodt, and RC Kistler. **Phase coherence of optical waveguides**. *Journal of Lightwave Technology*, **12**(4):603–606, 1994. 33

[275] Yisu Yang, Yangjin Ma, Hang Guan, Yang Liu, Steven Danziger, Stewart Ocheltree, Keren Bergman, Tom Baehr-Jones, and Michael Hochberg. **Phase coherence length in silicon photonic platform**. *Optics Express*, **23**(13):16890–16902, 2015. 33

[276] Lukas Chrostowski, Xu Wang, Jonas Flueckiger, Yichen Wu, Yun Wang, and Sahba Talebi Fard. **Impact of fabrication non-uniformity on chip-scale silicon photonic integrated circuits**. In *Optical Fiber Communication Conference*, pages Th2A–37. Optical Society of America, 2014. 33

[277] Hang Guan, Yangjin Ma, Ruizhi Shi, Ari Novack, Jingcheng Tao, Qing Fang, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg. **Ultra-compact silicon-on-insulator polarization rotator for polarization-diversified circuits**. *Optics Letters*, **39**(16):4703–4706, 2014. 34

[278] Yurii A Vlasov and Sharee J McNab. **Losses in single-mode silicon-on-insulator strip waveguides and bends**. *Optics Express*, **12**(8):1622–1631, 2004. 34

[279] Wim Bogaerts and SK Selvaraja. **Compact single-mode silicon hybrid rib/strip waveguide with adiabatic bends**. *IEEE Photonics Journal*, **3**(3):422–432, 2011. 34

[280] Takeshi Fujisawa, Shuntaro Makino, Takanori Sato, and Kunimasa Saitoh. **Low-loss, compact, and fabrication-tolerant Si-wire 90 waveguide bend using clothoid and normal curves for large scale photonic integrated circuits**. *Optics Express*, **25**(8):9150–9159, 2017. 34

[281] Tom Baehr-Jones, Thierry Pinguet, Patrick Lo Guo-Qiang, Steven Danziger, Dennis Prather, and Michael Hochberg. **Myths and rumours of silicon photonics**. *Nature Photonics*, **6**(4):206–208, 2012. 45

[282] Adithyaram Narasimha, Sherif Abdalla, Colin Bradbury, Aaron Clark, Jim Clymore, James Coyne, Anders Dahl, Steffen Gloeckner, Alberto Gruenberg, Drew Guckenberger, et al. **An ultra low power CMOS photonics technology platform for H/S optoelectronic transceivers at less than 1 dollar per Gbps**. In *Optical Fiber Communication Conference*, page OMV4. Optical Society of America, 2010. 45

[283] CR Doerr, L Chen, LL Buhl, and YK Chen. **8-Channel SiO2/Si3N4/Si/Ge CWDM Receiver**. *IEEE Photonics Technology Letters*, 2011. 46

[284] Long Chen, Christopher R Doerr, and Young-kai Chen. **Polarization-diversified DWDM receiver on silicon free of polarization-dependent wavelength shift**. In *Optical Fiber Communication Conference*, pages OW3G–7. Optical Society of America, 2012. 46, 50

[285] Dazeng Feng, Wei Qian, Hong Liang, Ning-Ning Feng, Shirong Liao, Cheng-Chih Kung, Joan Fong, Yong Liu, Roshanak Shafiiha, Daniel C Lee, et al. **Terabit/s single chip WDM receiver on the SOI platform**. In *Group IV Photonics (GFP), 2011 8th IEEE International Conference on*, pages 320–322. IEEE, 2011. 46

[286] Peter De Heyn, Jeroen De Coster, Peter Verheyen, Guy Lepage, Marianna Pantouvaki, Philippe Absil, Wim Bogaerts, Dries Van Thourhout, and Joris Van Campenhout. **Polarization-insensitive 5× 20Gb/s WDM Ge receiver using compact Si ring filters with collective thermal tuning**. In *Optical Fiber Communications Conference*, pages 1–3. IEEE, 2014. 46, 50

[287] Ari Novack, Mike Gould, Yisu Yang, Zhe Xuan, Matthew Streshinsky, Yang Liu, Giovanni Capellini, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, et al. **Germanium photodetector with 60 GHz bandwidth using inductive gain peaking**. *Optics Express*, **21**(23):28387–28393, 2013. 46

[288] CR Doerr, L Chen, LL Buhl, and Y-K Chen. **Eight-Channel SiO _2/Si _3 N _4/Si/Ge CWDM Receiver**. *IEEE Photonics Technology Letters*, **23**(17):1201–1203, 2011. 50

[289] Daniel Y Lee, Xuezhe Zheng, Jin Yao, Ying Luo, Jin-Hyoung Lee, Shiyun Lin, Hiren Thacker, Jock Bovington, Ivan Shubin, Stevan S Djordjevic, et al. **Error-free operation of a polarization-insensitive 4λ x 25 Gbps silicon photonic WDM receiver with closed-loop thermal stabilization of Si microrings**. *Optics Express*, **24**(12):13204–13209, 2016. 50

[290] Robert Gatdula, Kwangwoong Kim, Argishti Melikyan, Young-Kai Chen, and Po Dong. **Simultaneous four-channel thermal adaptation of polarization insensitive silicon photonics WDM receiver**. *Optics Express*, **25**(22):27119–27126, 2017. 50

[291] Michael Hochberg and Tom Baehr-Jones. **Towards fabless silicon photonics**. *Nature Photonics*, **4**(8):492–494, 2010. 52

[292] David Thomson, Aaron Zilkie, John E Bowers, Tin Komljenovic, Graham T Reed, Laurent Vivien, Delphine Marris-Morini, Eric Cassan, Léopold Virot, Jean-Marc Fédéli, et al. **Roadmap on silicon photonics**. *Journal of Optics*, **18**(7):073003, 2016. 52

[293] Anand Ramaswamy, Jonathan Roth, Erik Norberg, Robert S Guzzon, Jaehyuk Shin, Jeff Imamura, Brian Koch, Daniel Sparacin, Greg Fish, Benjamin G Lee, et al. **A WDM 4x28Gbps integrated silicon photonic transmitter driven by 32nm CMOS driver ICs**. In *Optical Fiber Communication Conference*, pages Th5B–5. Optical Society of America, 2015. 52

[294] Rodolfo E Camacho-Aguilera, Yan Cai, Neil Patel, Jonathan T Bessette, Marco Romagnoli, Lionel C Kimerling, and Jurgen Michel. **An electrically pumped germanium laser**. *Optics Express*, **20**(10):11316–11320, 2012. 52

[295] Stephan Wirths, Richard Geiger, N Von Den Driesch, G Mussler, T Stoica, S Mantl, Z Ikonic, Ml Luysberg, S Chiussi, JM Hartmann, et al. **Lasing in direct-bandgap GeSn alloy grown on Si**. *Nature Photonics*, **9**(2):88, 2015. 52

[296] Siming Chen, Wei Li, Jiang Wu, Qi Jiang, Mingchu Tang, Samuel Shutts, Stella N Elliott, Angela Sobiesierski, Alwyn J Seeds, Ian Ross, et al. **Electrically pumped continuous-wave III–V quantum dot lasers on silicon**. *Nature Photonics*, **10**(5):307–311, 2016. 52

[297] Alan Y Liu, Chong Zhang, Justin Norman, Andrew Snyder, Dmitri Lubyshev, Joel M Fastenau, Amy WK Liu, Arthur C Gossard, and John E Bowers. **High performance continuous wave 1.3 μ m quantum dot lasers on silicon**. *Applied Physics Letters*, **104**(4):041104, 2014. 52

[298] Emir Salih Magden, Nanxi Li, Jonathan DB Bradley, Neetesh Singh, Alfonso Ruocco, Gale S Petrich, Gerald Leake, Douglas D Coolbaugh, Erich P Ippen, Michael R Watts, et al. **Monolithically-integrated distributed feedback laser compatible with CMOS processing**. *Optics Express*, **25**(15):18058–18065, 2017. 52

[299] Shahram Keyvaninia, Gunther Roelkens, Dries Van Thourhout, Christophe Jany, Marco Lamponi, Alban Le Liepvre, Francois Lelarge, Dalila Make, Guang-Hua Duan, Damien Bordel, et al. **Demonstration of a heterogeneously integrated III-V/SOI single wavelength tunable laser**. *Optics Express*, **21**(3):3784–3792, 2013. 52, 66

[300] JC Hulme, JK Doylend, and JE Bowers. **Widely tunable Vernier ring laser on hybrid silicon**. *Optics Express*, **21**(17):19718–19722, 2013. 52

[301] Timothy Creazzo, Elton Marchena, Stephen B Krasulick, KL Paul, Derek Van Orden, John Y Spann, Christopher C Blivin, Lina He, Hong Cai, John M Dallesasse, et al. **Integrated tunable CMOS laser**. *Optics Express*, **21**(23):28048–28053, 2013. 52, 61, 66

[302] Tao Chu, Nobuhide Fujioka, and Masashige Ishizaka. **Compact, lower-power-consumption wavelength tunable laser fabricated with silicon photonic wire waveguide micro-ring resonators**. *Optics Express*, **17**(16):14063–14068, 2009. 52

[303] AJ Zilkie, P Seddighian, BJ Bijlani, W Qian, DC Lee, S Fathololoumi, J Fong, R Shafiiha, D Feng, BJ Luff, et al. **Power-efficient III-V/Silicon external cavity DBR lasers**. *Optics Express*, **20**(21):23456–23462, 2012. 52, 59

[304] Shinsuke Tanaka, Seok-Hwan Jeong, Shigeaki Sekiguchi, Teruo Kurahashi, Yu Tanaka, and Ken Morito. **High-output-power, single-wavelength silicon hybrid laser using precise flip-chip bonding technology**. *Optics Express*, **20**(27):28057–28069, 2012. 52, 66

REFERENCES

[305] RM Oldenbeuving, EJ Klein, Herman L Offerhaus, Christopher James Lee, H Song, and Klaus J Boller. **25 kHz narrow spectral bandwidth of a wavelength tunable diode laser with a short waveguide-based external cavity**. *Laser Physics Letters*, **10**(1):015804, 2012. 52

[306] Bradley Snyder, Brian Corbett, and Peter O'Brien. **Hybrid integration of the wavelength-tunable laser with a silicon photonic integrated circuit**. *Journal of Lightwave Technology*, **31**(24):3934–3942, 2013. 52

[307] Shuyu Yang, Yi Zhang, David W Grund, Garret A Ejzak, Yang Liu, Ari Novack, Dennis Prather, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, et al. **A single adiabatic microring-based laser in 220 nm silicon-on-insulator**. *Optics Express*, **22**(1):1172–1180, 2014. 52

[308] Yi Zhang, Shuyu Yang, Hang Guan, Andy Eu-Jin Lim, Guo-Qiang Lo, Peter Magill, Tom Baehr-Jones, and Michael Hochberg. **Sagnac loop mirror and micro-ring based laser cavity for silicon-on-insulator**. *Optics Express*, **22**(15):17872–17879, 2014. 52, 53

[309] Jin Hyoung Lee, Ivan Shubin, Jin Yao, Justin Bickford, Ying Luo, Shiyun Lin, Stevan S Djordjevic, Hiren D Thacker, John E Cunningham, Kannan Raj, et al. **High power and widely tunable Si hybrid external-cavity laser for power efficient Si photonics WDM links**. *Optics Express*, **22**(7):7678–7685, 2014. 52

[310] Bowen Song, Cristian Stagarescu, Sasa Ristic, Alex Behfar, and Jonathan Klamkin. **3D integrated hybrid silicon laser**. *Optics Express*, **24**(10):10435–10444, 2016. 52

[311] Shiyun Lin, Xuezhe Zheng, Jin Yao, Stevan S Djordjevic, John E Cunningham, Jin-Hyoung Lee, Ivan Shubin, Ying Luo, Jock Bovington, Daniel Y Lee, et al. **Efficient, tunable flip-chip-integrated III-V/Si hybrid external-cavity laser array**. *Optics Express*, **24**(19):21454–21462, 2016. 52

[312] Bin Liu, Ali Shakouri, and John E Bowers. **Wide tunable double ring resonator coupled lasers**. *IEEE Photonics Technology Letters*, **14**(5):600–602, 2002. 52

[313] Shinji Matsuo and Toru Segawa. **Microring-resonator-based widely tunable lasers**. *IEEE Journal of Selected Topics in Quantum Electronics*, **15**(3):545–554, 2009. 52

[314] Yang Liu, Ran Ding, Yangjin Ma, Yisu Yang, Zhe Xuan, Qi Li, Andy Eu-Jin Lim, Guo-Qiang Lo, Keren Bergman, Tom Baehr-Jones, et al. **Silicon Mod-MUX-Ring transmitter with 4 channels at 40 Gb/s**. *Optics Express*, **22**(13):16431–16438, 2014. 55

[315] Amnon Yariv. **Universal relations for coupling of optical power between microresonators and dielectric waveguides**. *Electronics Letters*, **36**(4):321–322, 2000. 55

[316] Xuezhe Zheng, Shiyun Lin, Ying Luo, Jin Yao, Guoliang Li, Stevan S Djordjevic, Jin-Hyoung Lee, Hiren D Thacker, Ivan Shubin, Kannan Raj, et al. **Efficient WDM laser sources towards terabyte/s silicon photonic interconnects**. *Journal of Lightwave Technology*, **31**(24):4142–4154, 2013. 58

[317] Jin-Hyoung Lee, Jock Bovington, Ivan Shubin, Ying Luo, Jin Yao, Shiyun Lin, John E Cunningham, Kannan Raj, Ashok V Krishnamoorthy, and Xuezhe Zheng. **Demonstration of 12.2% wall plug efficiency in uncooled single mode external-cavity tunable Si/III-V hybrid laser**. *Optics Express*, **23**(9):12079–12088, 2015. 58

[318] Jin-Hyoung Lee, Daniel Y Lee, Ivan Shubin, Jock Bovington, Stevan S Djordjevic, Shiyun Lin, Ying Luo, Jin Yao, John E Cunningham, Kannan Raj, et al. **III-V/Si hybrid laser stabilization using micro-ring feedback control**. *IEEE Photonics Journal*, **8**(5):1–7, 2016. 59

[319] Tam N Huynh, Lim Nguyen, and Liam P Barry. **Phase noise characterization of SGDBR lasers using phase modulation detection method with delayed self-heterodyne measurements**. *Journal of Lightwave Technology*, **31**(8):1300–1308, 2013. 61

[320] Shiyu Li, Di Zhang, Jianyi Zhao, Qi Yang, Xi Xiao, Shenglei Hu, Lei Wang, Miaofeng Li, Xuesheng Tang, Ying Qiu, et al. **Silicon micro-ring tunable laser for coherent optical communication**. *Optics Express*, **24**(6):6341–6349, 2016. 62

[321] Yi Hu, Wei Cao, Xuesheng Tang, Weidong Ma, Ying Qiu, Shiyu Li, and Shaohua Yu. **High power, high SMSR and wide tuning range silicon micro-ring tunable laser**. *Optics Express*, **25**(7):8029–8035, 2017. 66

[322] Brian Stern, Xingchen Ji, Avik Dutt, and Michal Lipson. **Compact narrow-linewidth integrated laser based on a low-loss silicon nitride ring resonator**. *Optics Letters*, **42**(21):4541–4544, 2017. 66

[323] Peter Kogge and John Shalf. **Exascale Computing Trends: Adjusting to the" New Normal" for Computer Architecture**. *Computing in Science & Engineering*, **15**(6):16–26, 2013. 69

[324] Sally A McKee. **Reflections on the memory wall**. In *Proceedings of the 1st conference on Computing frontiers*, page 162. ACM, 2004. 69, 71

[325] David AB Miller. **Rationale and challenges for optical interconnects to electronic chips**. *Proceedings of the IEEE*, **88**(6):728–749, 2000. 69

[326] John M Shalf and Robert Leland. **Computing beyond moore's law**. *Computer*, **48**(12):14–23, 2015. 70

[327] Ke Wen, Sébastien Rumley, Payman Samadi, Christine P Chen, and Keren Bergman. **Silicon photonics in post Moores Law era: technological and architectural implications**. In *Post-Moores Era Supercomputing (PMES) Workshop, Salt Lake City. IEEE*, 2016. 70

[328] Jianmin Chen, Xi Tao, Zhen Yang, Jih-Kwon Peir, Xiaoyuan Li, and Shih-Lien Lu. **Guided region-based GPU scheduling: utilizing multi-thread parallelism to hide memory latency**. In *Parallel & Distributed Processing (IPDPS), 2013 IEEE 27th International Symposium on*, pages 441–451. IEEE, 2013. 70

[329] Scott Beamer, Chen Sun, Yong-Jin Kwon, Ajay Joshi, Christopher Batten, Vladimir Stojanović, and Krste Asanović. **Re-architecting DRAM memory systems with monolithically integrated silicon photonics**. In *ACM SIGARCH Computer Architecture News*, **38**, pages 129–140. ACM, 2010. 70

[330] Gabriel H Loh. **3D-stacked memory architectures for multi-core processors**. In *Computer Architecture, 2008. ISCA'08. 35th International Symposium on*, pages 453–464. IEEE, 2008. 70

[331] Chen Sun, Mark T Wade, Yunsup Lee, Jason S Orcutt, Luca Alloatti, Michael S Georgas, Andrew S Waterman, Jeffrey M Shainline, Rimas R Avizienis, Sen Lin, et al. **Single-chip microprocessor that communicates directly using light**. *Nature*, **528**(7583):534–538, 2015. 70

[332] Chen Sun, Michael Georgas, Jason Orcutt, Benjamin Moss, Yu-Hsin Chen, Jeffrey Shainline, Mark Wade, Karan Mehta, Kareem Nammari, Erman Timurdogan, et al. **A monolithically-integrated chip-to-chip optical link in bulk CMOS**. *IEEE Journal of Solid-State Circuits*, **50**(4):828–844, 2015. 70, 71

[333] Yasuhiko Arakawa, Takahiro Nakamura, Yutaka Urino, and Tomoyuki Fujita. **Silicon photonics for next generation system integration platform**. *IEEE Communications Magazine*, **51**(3):72–77, 2013. 70

[334] Jason S Orcutt, Rajeev J Ram, and Vladimir Stojanović. **Integration of silicon photonics into electronic processes**. Society of Photo-Optical Instrumentation Engineers (SPIE), 2013. 70

[335] Xianshu Luo, Yuanbing Cheng, Junfeng Song, Tsung-Yang Liow, Qi Jie Wang, and Mingbin Yu. **Wafer-Scale Dies-Transfer Bonding Technology for Hybrid III/V-on-Silicon Photonic Integrated Circuit Application**. *IEEE Journal of Selected Topics in Quantum Electronics*, **22**(6):443–454, 2016. 70

[336] Meisam Bahadori, Sébastien Rumley, Robert Polster, Alexander Gazman, Matt Traverso, Mark Webster, Kaushik Patel, and Keren Bergman. **Energy-performance optimized design of silicon photonic interconnection networks for high-performance computing**. In *2017 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 326–331. IEEE, 2017. 70

[337] Benjamin G Lee, Aleksandr Biberman, Po Dong, Michal Lipson, and Keren Bergman. **All-optical comb switch for multiwavelength message routing in silicon photonic networks**. *IEEE Photonics Technology Letters*, **20**(10):767–769, 2008. 71

[338] Po Dong, Stefan F Preble, and Michal Lipson. **All-optical compact silicon comb switch**. *Optics Express*, **15**(15):9600–9605, 2007. 71

[339] Michael R Watts, William A Zortman, Douglas C Trotter, Ralph W Young, and Anthony L Lentine. **Vertical junction silicon microdisk modulators and switches**. *Optics Express*, **19**(22):21989–22003, 2011. 71

[340] Christopher Batten, Ajay Joshi, Jason Orcutt, Anatol Khilo, Benjamin Moss, Charles W Holzwarth, Miloš A Popovic, Hanqing Li, Henry I Smith, Judy L Hoyt, et al. **Building many-core processor-to-DRAM networks with monolithic CMOS silicon photonics**. *IEEE Micro*, **29**(4), 2009. 71

[341] Yan Pan, Prabhat Kumar, John Kim, Gokhan Memik, Yu Zhang, and Alok Choudhary. **Firefly: Illuminating future network-on-chip with nanophotonics**. In *ACM SIGARCH Computer Architecture News*, **37**, pages 429–440. ACM, 2009. 71

[342] Dana Vantrease, Robert Schreiber, Matteo Monchiero, Moray McLaren, Norman P Jouppi, Marco Fiorentino, Al Davis, Nathan Binkert, Raymond G Beausoleil, and Jung Ho Ahn. **Corona: System implications of emerging nanophotonic technology**. In *ACM SIGARCH Computer Architecture News*, **36**, pages 153–164. IEEE Computer Society, 2008. 71

[343] Michele Petracca, Benjamin G Lee, Keren Bergman, and Luca P Carloni. **Design exploration of optical interconnection networks for chip multiprocessors**. In *High Performance Interconnects, 2008. HOTI'08. 16th IEEE Symposium on*, pages 31–40. IEEE, 2008. 71

[344] Hang Guan, Sébastien Rumley, Ke Wen, David Donofrio, John Shalf, and Keren Bergman. **Reconfigurable Silicon Photonic Interconnect for Many-Core Architecture**. In *International Conference on High Performance Computing*, pages 89–97. Springer, 2017. 71

[345] Daniel Brunina, Xiaoliang Zhu, Kishore Padmaraju, Long Chen, Michal Lipson, and Keren Bergman. **10-Gb/s WDM optically-connected memory system using silicon microring modulators**. In *European Conference and Exhibition on Optical Communication*, pages Mo–2. Optical Society of America, 2012. 71

[346] Takashi Shiraishi, Qi Li, Yang Liu, Xiaoliang Zhu, Kishore Padmaraju, Ran Ding, Michael Hochberg, and Keren Bergman. **A reconfigurable and redundant optically-connected memory system using a silicon photonic switch**. In *Optical Fiber Communications Conference*, pages 1–3. IEEE, 2014. 71

[347] P Maniotis, D Fitsios, GT Kanellos, and N Pleros. **Optical buffering for chip multiprocessors: a 16GHz optical cache memory architecture**. *Journal of Lightwave Technology*, **31**(24):4175–4191, 2013. 71

[348] Jagan Jayaraj, Arun F Rodrigues, Simon D Hammond, and Gwendolyn R Voskuilen. **The potential and perils of multi-level memory**. In *Proceedings of the 2015 International Symposium on Memory Systems*, pages 191–196. ACM, 2015. 72

[349] Avinash Sodani, Roger Gramunt, Jesus Corbal, Ho-Seop Kim, Krishna Vinod, Sundaram Chinthamani, Steven Hutsell, Rajat Agarwal, and Yen-Chen Liu. **Knights landing: Second-generation intel xeon phi product**. *IEEE Micro*, **36**(2):34–46, 2016. 72

[350] Shigeru Nakamura, Shigeki Takahashi, Masahiro Sakauchi, Tomoyuki Hino, Mingbin Yu, and Guoqiang Lo. **Wavelength selective switching with one-chip silicon photonic circuit including 8 x 8 matrix switch**. In *Optical Fiber Communication Conference*, page OTuM2. Optical Society of America, 2011. 76

REFERENCES

[351] Colm Browning, Kai Shi, Andrew D Ellis, and Liam P Barry. **Optical burst-switched SSB-OFDM using a fast switching SG-DBR laser**. *Journal of Optical Communications and Networking*, **5**(9):994–1000, 2013. 76

[352] Arun F Rodrigues, K Scott Hemmert, Brian W Barrett, Chad Kersey, Ron Oldfield, Marlo Weston, R Risen, Jeanine Cook, Paul Rosenfeld, E CooperBalls, et al. **The structural simulation toolkit**. *ACM SIGMETRICS Performance Evaluation Review*, **38**(4):37–42, 2011. 77

[353] Kishore Padmaraju, Dylan F Logan, Takashi Shiraishi, Jason J Ackert, Andrew P Knights, and Keren Bergman. **Wavelength locking and thermally stabilizing microring resonators using dithering signals**. *Journal of Lightwave Technology*, **32**(3):505–512, 2014. 83

[354] David Calhoun, Qi Li, Colm Browning, Nathan C Abrams, Yang Liu, Ran Ding, Liam P Barry, Thomas W Baehr-Jones, Michael Hochberg, and Keren Bergman. **Programmable wavelength locking and routing in a silicon-photonic interconnection network implementation**. In *Optical Fiber Communication Conference*, pages Tu2H–3. Optical Society of America, 2015. 83

[355] Alexander Gazman, Colm Browning, Meisam Bahadori, Ziyi Zhu, Payman Samadi, Sébastien Rumley, Vidak Vujicic, Liam P Barry, and Keren Bergman. **Software-defined control-plane for wavelength selective unicast and multicast of optical data in a silicon photonic platform**. *Optics Express*, **25**(1):232–242, 2017. 83

[356] Farzad Fatollahi-Fard, David Donofrio, George Michelogiannakis, and John Shalf. **Opensoc fabric: On-chip network generator: Using chisel to generate a parameterizable on-chip interconnect fabric**. In *Proceedings of the 2014 International Workshop on Network on Chip Architectures*, pages 45–50. ACM, 2014. 84

[357] James F Kurose and Keith W Ross. *Computer networking: a top-down approach*. Addison-Wesley Reading, 2010. 85

[358] Li Zhu, Weijian Yang, and Connie Chang-Hasnain. **Very high efficiency optical coupler for silicon nanophotonic waveguide and single mode optical fiber**. *Optics Express*, **25**(15):18462–18473, 2017. 89

Appendix
Relevant Author Publications

- **H. Guan**, A. Novack, T. Galfsky, Y. Ma, S. Fathololoumi, A. Horth, T. N. Huynh, J. Roman, Y. Liu, T. Baehr-Jones, K. Bergman, M. Hochberg **Widely-tunable, narrow-linewidth III-V/silicon hybrid external-cavity laser for coherent communication.** Optics Express, 26 (6), 2018.

- **H. Guan**, Y. Ma, R. Shi, X. Zhu, R. Younce, Y. Chen, J. Roman, N. Ophir, Y. Liu, R. Ding, T. Baehr-Jones, K. Bergman, M. Hochberg. **Compact and low loss 90° optical hybrid on a silicon-on-insulator platform.** Optics Express, 25 (23), 2017.

- **H. Guan**, S. Rumley, K. Wen, D. Donofrio, J. Shalf, K. Bergman. **Reconfigurable silicon photonic interconnect for many-core architecture.** HCPM 2017 : Workshop on HPC Computing in a Post Moore's Law World 2017, Frankfurt, 2017.

- **H. Guan**, A. Gazman, Y. Ma, Y. Liu, Q. Li, R. Ding, Y. Li, X. Zhu, T. Baehr-Jones, M. Hochberg, K. Bergman. **Polarization-insensitive 40Gb/s 4-WDM channels receiver on SOI platform.** Optical Interconnects Conference, San Diego, 2015.

- **H. Guan**, A. Novack, M. Streshinsky, R.Shi, Q. Fang, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, M. Hochberg. **CMOS-compatible highly efficient polarization splitter and rotator based on a double-etched directional coupler.** Optics Express, 22 (3), 2014.

- **H. Guan**, Y. Ma, R. Shi, A. Novack, J. Tao, Q. Fang, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, M. Hochberg. **Ultracompact silicon-on-insulator polarization rotator for polarization-diversified circuits.** Optics Letters, 39 (16), 2014.

REFERENCES

- **H. Guan**, A. Novack, M. Streshinsky, R. Shi, Y. Liu, Q. Fang, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, M. Hochberg. **High-efficiency low-crosstalk 1310-nm polarization splitter and rotator built on a SOI platform.** IEEE Photonics Technology Letters, 26 (9), 2014.

- **H. Guan**, Q. Fang, G.-Q. Lo, K. Bergman. **A high-efficiency bi-wavelength polarization splitter-rotator on the SOI platform.** IEEE Photonics Technology Letters, 27 (5), 2014.

- A. Novack, M. Streshinsky, T. Huynh, T. Galfsky, **H. Guan**, Y. Liu, Y. Ma, R. Shi, A. Horth, Y. Chen, A. Hanjani, J. Roman, Y. Dziashko, R. Ding, S. Fathololoumi, A. E.-J. Lim, K. Padmaraju, R. Sukkar, R. Younce, H. Rohde, R. Palmer, G. Saathoff, T. Wuth, M. Bohn, A. Ahmed, M. Ahmed, C. Williams, D. Lim, A. Elmoznine, A. Rylyakov, T. Baehr-Jones, P. Magill, D. Scordo, and M. Hochberg **A silicon photonic transceiver and hybrid tunable laser for 64 Gbaud coherent communication.** Optical Fiber Conference (OFC), San Diego, 2018.

- D. Zhuo, K. X. Zou, M. Ghobadi, R. Mahajan, A. Phanishayee, **H. Guan**, A. Krishnamurthy, T. Anderson. **RAIL: a case for redundant arrays of inexpensive links in data center networks.** 14th USENIX Symposium on Networked Systems Design and Implementation, 2017.

- K. Wen, **H. Guan**, D. M. Calhoun, S. Rumley, D. Donofrio, J. Shalf, K. Bergman. **Silicon photonic memory interconnect for many-core architectures.** High Performance Extreme Computing Conference, Waltham, 2016.

- Y. Ma, Y. Liu, Q. Li, R. Ding, T. Baehr-Jones, P. Magill, **H. Guan**, A. Gazman, Q. Li, K. Bergman, M. Hochberg. **Optimized silicon photonic components for high-performance interconnect systems.** Photonics Conference, 2015.

- P. Samadi, **H. Guan**, K. Wen, K. Bergman. **A software-defined optical gateway for converged inter/intra data center networks.** Optical Interconnects Conference, San Diego, 2015.

- P. Samadi, J. Xu, K. Wen, **H. Guan**, Z. Li, K. Bergman. **Experimental demonstration of converged inter/intra data center network architecture.** 17th International Conference on Transparent Optical Networks, Boston, 2015.

- Y. Ma, Y. Liu, **H. Guan**, A. Gazman, Q. Li, R. Ding, Y. Li, K. Bergman, T. Baehr-Jones, and M. Hochberg. **Symmetrical polarization splitter/rotator design and application in a polarization insensitive WDM receiver.** Optics Express, 23 (12), 2015.

- Y. Yang, Y. Ma, **H. Guan**, Y. Liu, S. Danziger, S. Ocheltree, K. Bergman, T. Baehr-Jones, M. Hochberg . **Phase coherence length in silicon photonic platform.** Optics Express, 22 (13), 2015.

- Y. Zhang, S. Yang, X. Zhu, Q. Li, **H. Guan**, P. Magill, K. Bergman, T. Baehr-Jones, M. Hochberg. **Quantum dot SOA/silicon external cavity multi-wavelength laser.** Optics Express, 23 (4), 2015.

- Y. Zhang, S. Yang, **H. Guan**, A. E.-J. Lim, G.-Q. Lo, P. Magill, T. Baehr-Jones, M. Hochberg. **Sagnac loop mirror and micro-ring based laser cavity for silicon-on-insulator.** Optics Express, 22 (15), 2014.

- R. Shi, **H. Guan**, A. Novack, M. Streshinsky, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, M. Hochberg. **High-efficiency grating couplers near 1310 nm fabricated by 248 nm DUV lithography.** IEEE Photonics Technology Letters, 26 (15), 2014.